

PART 1

**THE TRANSPUTER
FAMILY**

Transputer Family Strategy

Transputer 5 Point Strategy

- 1 **Low Cost - T400 and plastic packaging**
- 2 **Next Generations - Hxx and Exx**
- 3 **Enhance / Customize - ASIC Macrocells**
- 4 **Target Growth Markets - S/W and H/W**
- 5 **iq systems for prototyping and OEM**

INMOS Product Family

SRAMs

Broad range of fast static RAMs. 4K to 256K, x1 to x8, 15 to 70ns. 1 & 4M planned.

Transputer

Family of 16 and 32 bit microprocessors for fast, powerful multi processing

iq systems

A family of modular board level products and application software.

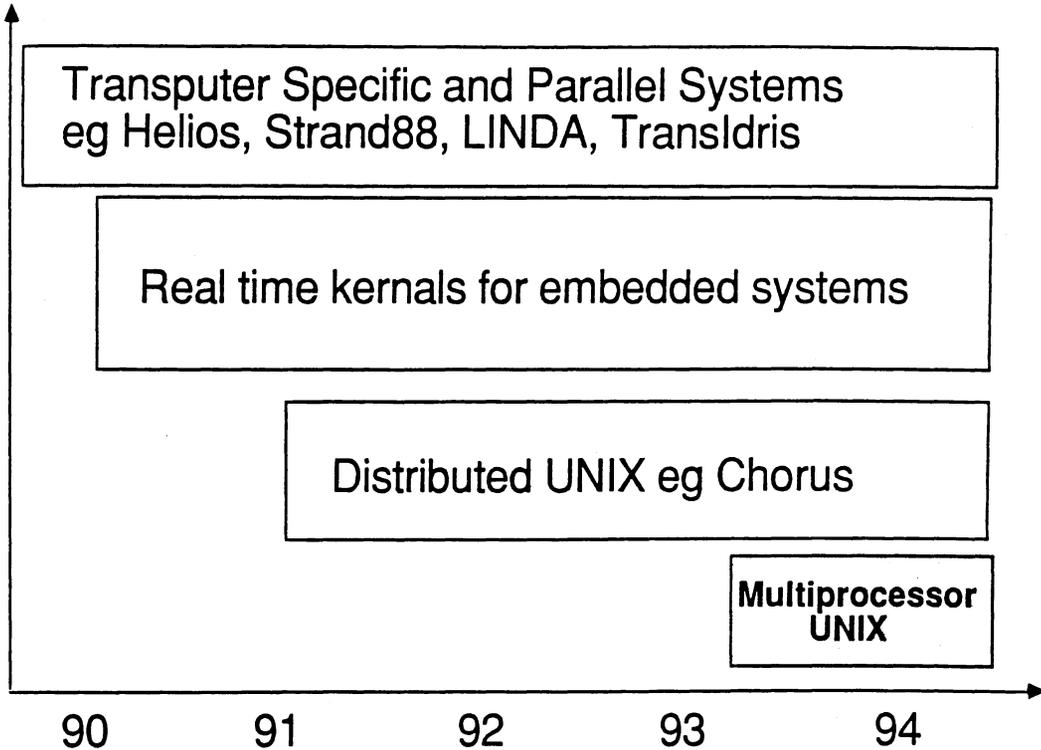
Graphics

Colour Look Up Tables - PC standard. High performance Colour Video Controllers

Low Cost Transputers

- T400 - Introduced at *2\$ per MIPS* Sept 89.
- T400 makes 32 bit processors and multiprocessing cost effective for volume production.
- Low cost surface mount packaging.
PQFP for Japan and PLCC options.
- T400 designed to be the first ASIC core

Operating Systems



Transputer Target Applications



Office Automation

Telecoms

Page Printers
X-Windows
Terminals
Fax Machines
Disk Arrays

PC & Workstations

Application Accelerators
Graphics/Display
Supercomputers

Network Management
Datacomms
Telephone Exchanges
Satellites

Control

Radar/Sonar
Missiles + Smart Weapons
Avionics
Simulators

Robotics
Machine Control
Factory Automation
Medical Imaging

Military



TFS A 008



GPS (Global Positioning by Satellite)

Emerging Market.

Worldwide TAM growing to 500ku by 1995

Could be 1.5Mu if adopted in cars.

Satellites available and costs decreasing.

Transputer solution eliminates need for dedicated DSP hardware. Minimizes time to market

INMOS have complete system solution with h/w and licensable s/w.



TFS A 009

X- Terminals

Market projected to grow from 200ku to 1Mu in 1993

Application requires high performance for
Networks, X-Protocol, and graphics

Primary target is upgrade of VT100.

Transputers meet X-Terminal model of communicating
sequential processes.

Transputers offer scaleable performance for range of
low to high end terminals.

Disk Arrays

Problems with single drives :

- Transfer speed, Capacity, Access time, Fault tolerance

Applications in servers, networks and fault tolerant systems

Transputers have high comms b/width with low overheads

Transputers can offer intelligence for backups, and file searches

**SCSI software and hardware solution
available today.**

Office Automation - Page Printers

- Fastest growth application for for 32 bit uP's.
32 bit TAM = 140Ku 1988 → 4.8Mu in 1993. (x30)
- Transition from 300 DPI mono to 600 DPI full colour.
Full colour requires large memory capacity.
over 80% of system cost.
- Transputers offer scalable performance. Software
available to support transputer.
- Communications and multiprocessing support banded
postscript architecture for future development.

Transputer

Customer Support

TRANSPUTER CUSTOMER SUPPORT



● RTC's - 50 PEOPLE

- 49 W/W SGS-THOMSON SALES OFFICES

- OVER 50 DISTRIBUTORS

- 13 CENTRES

Software - Support Network

- 1 **Inmos Business Centres**
Field Application Engineers (FAEs).
Day to day enquiries.
- 2 **Regional Transputer Centres**
Regional Transputer Engineers.
Customer related projects, benchmarks etc.
- 3 **Software Support**
Central Technology Group.
Guaranteed turnarounds.
New releases, bug fixes.
Direct line to software developers.
Electronic mail support.
- 4 **Distributor Support**

User's Groups

- Over 5000 members worldwide
- Includes both academic and industrial subscribers
- Forum for the interchange of information among existing and prospective users of INMOS products
- Groups established in Europe, North America, Australasia and Japan
- Newsletter and Technical papers published
- Conferences held twice yearly
- First Worldwide Meeting - California, April 1991

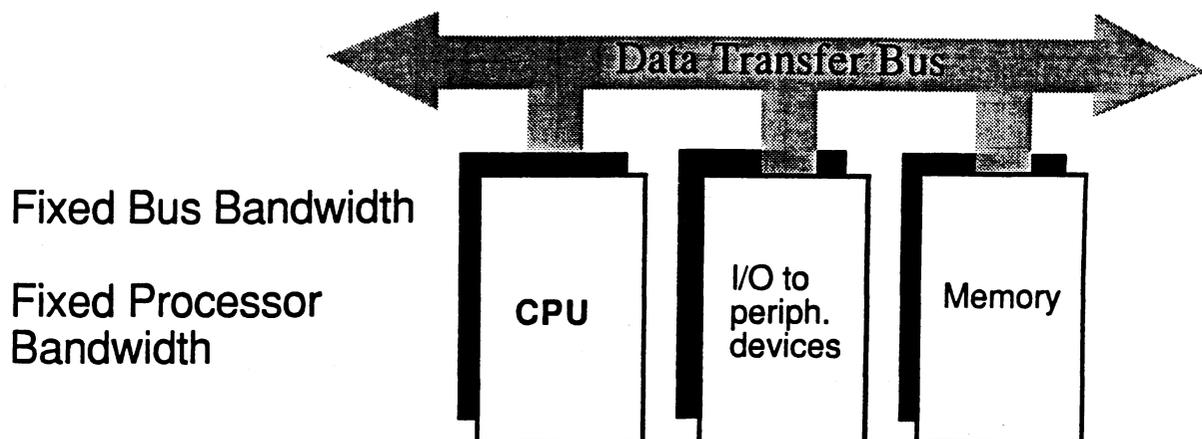
Literature Available

- Glossy Brochures
- Product Flyers
- Transputer Databooks
- Transputer Applications Notes

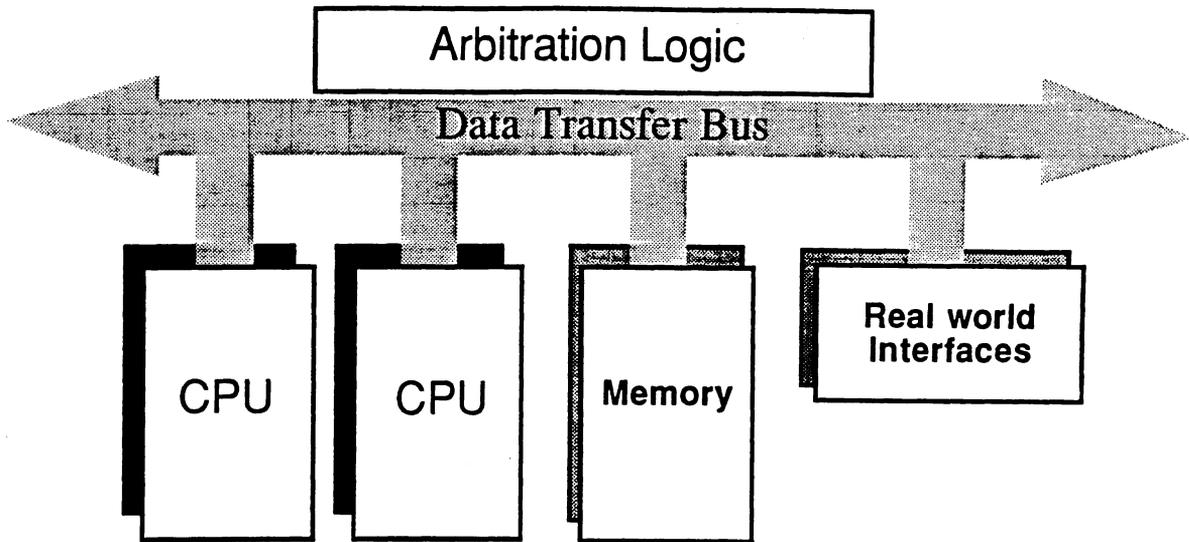
Transputer

The Concept

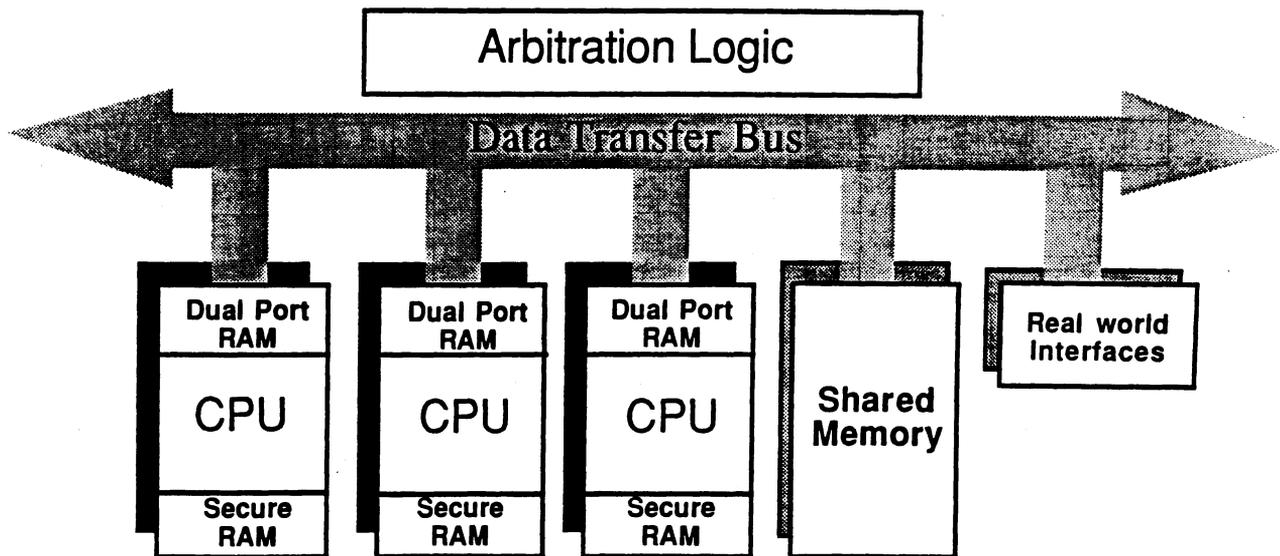
Traditional MICROPROCESSOR Architecture



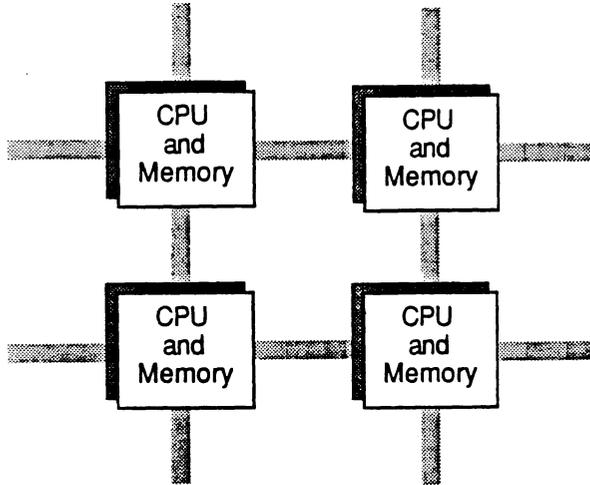
Traditional Multiprocessor Architecture - 1



Traditional Multiprocessor Architecture - 2



The Transputer



More Processor Bandwidth

More Comms Bandwidth

No arbitration Software

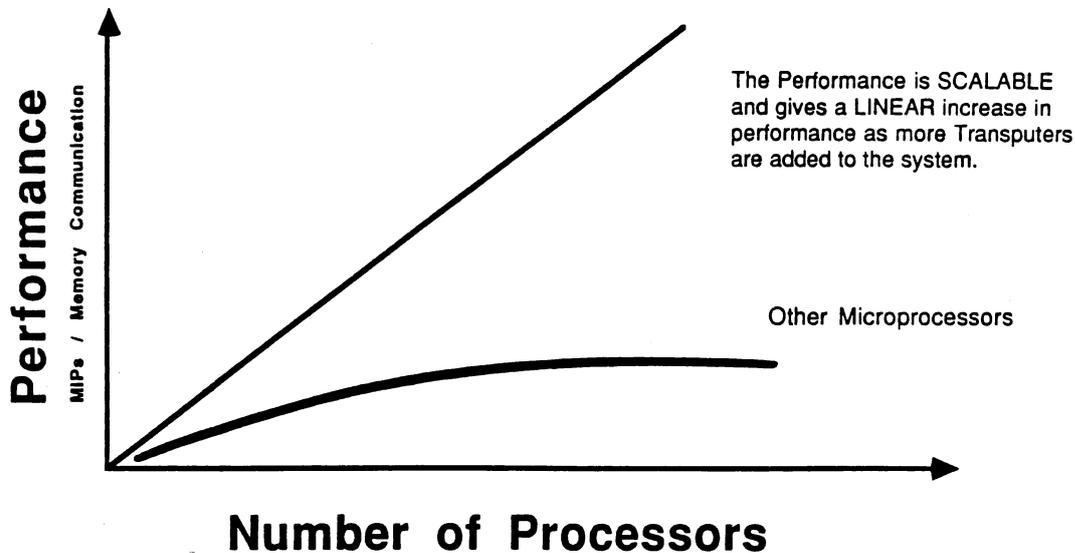
No arbitration Hardware

Transfer supported by CPU

Multiprocessing Made Simple !

Scalable Performance

10 transputers - 10 X Performance !



Generic Transputer

Fast CPU - best of RISC and CISC !

Fast On-Board Memory

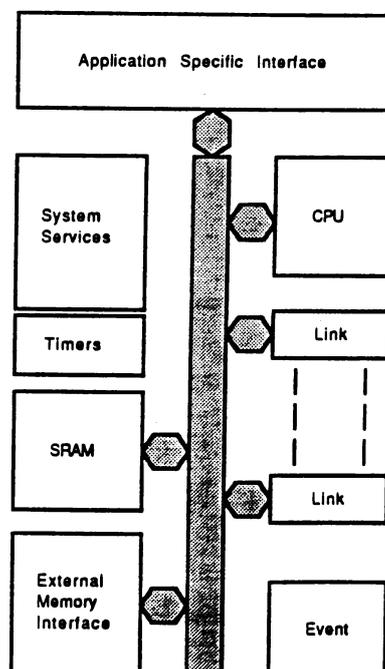
Hardware Support for concurrency

High speed Serial Links support multiprocessor operation

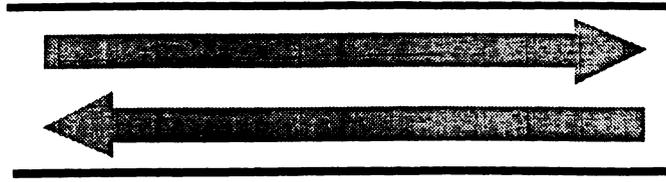
Virtual Timers

Minimum External Support circuitry

Simple System Engineering



Serial Link



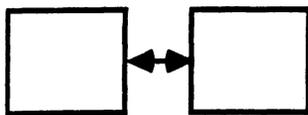
- Means of Interconnection between transputers.
 - Bidirectional.
 - Point-to-point.
- Speed Options : 5, 10, 20 Mbits/s.
- Can function independantly of CPU.

The Channel Concept

A Channel is :

- Point to point** Communication is from one process to another
- One Way** Use two channels for bi-directional transfer
- Unbuffered** Data is copied direct from one process to another
- Synchronised** Data is copied when both sender and receiver are ready

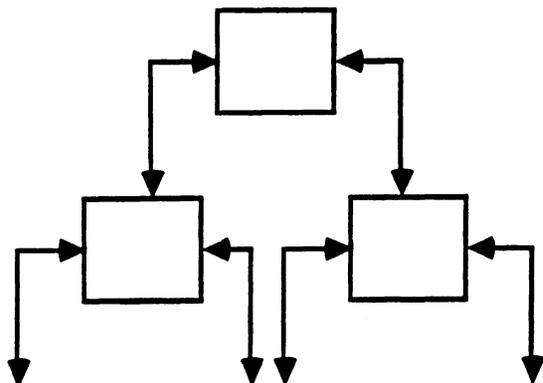
Connectivity



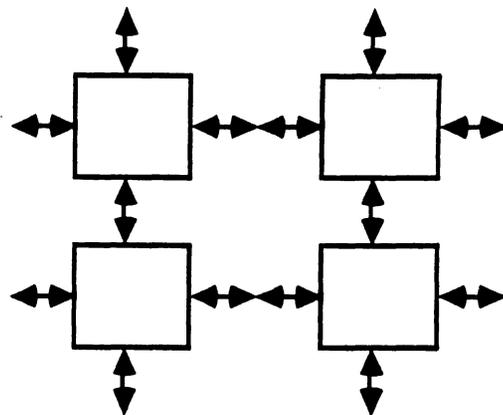
One link connects two transputers



Two links allow pipelines

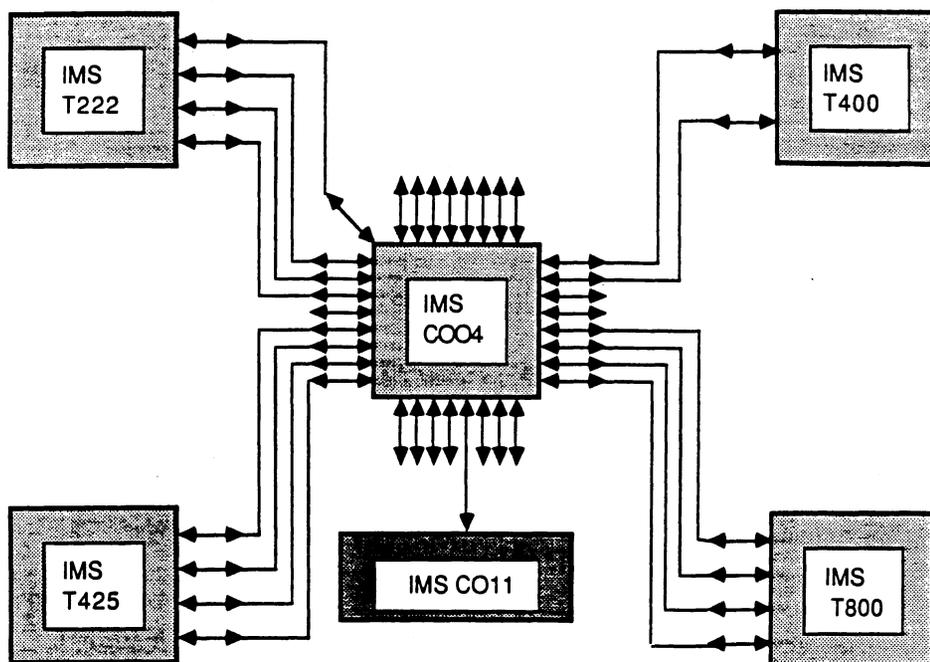


Three links for tree structures

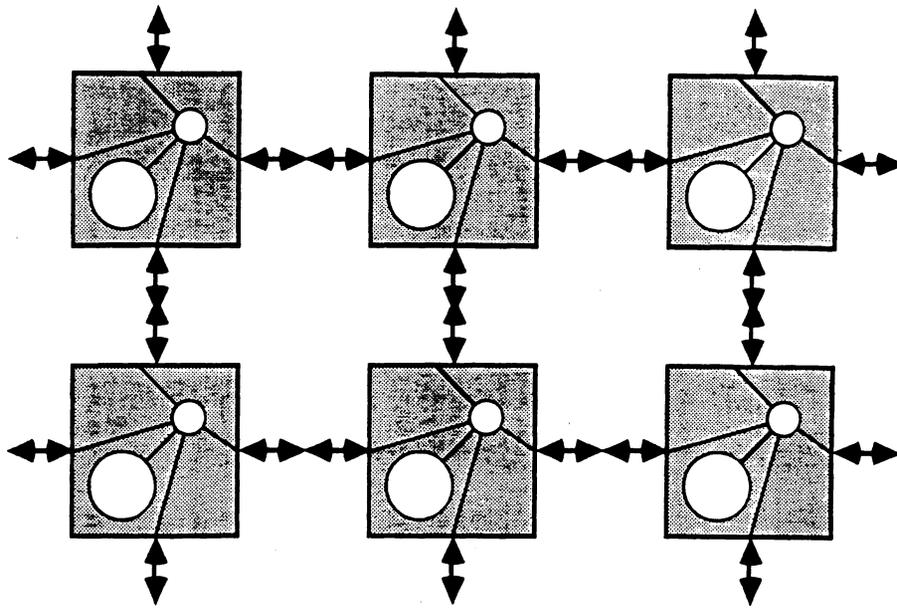


Four links for square arrays

IMS COO4 Link Switch

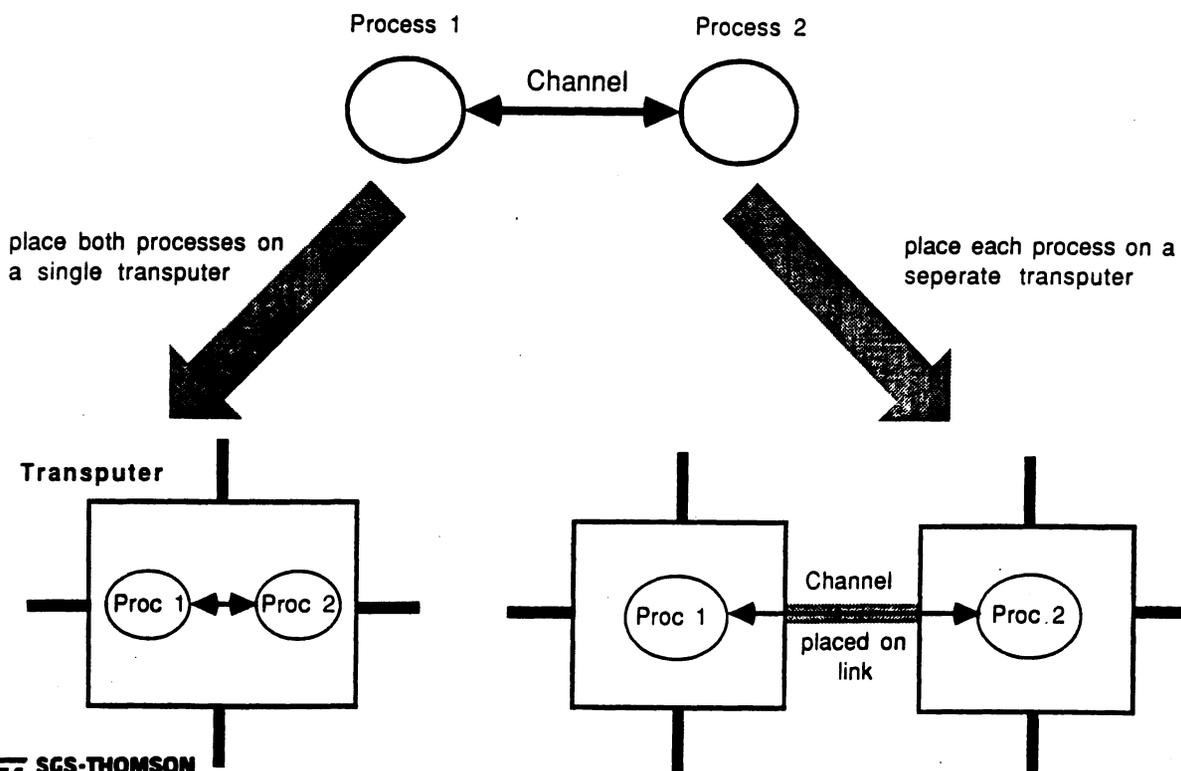


Multi-transputer Communication



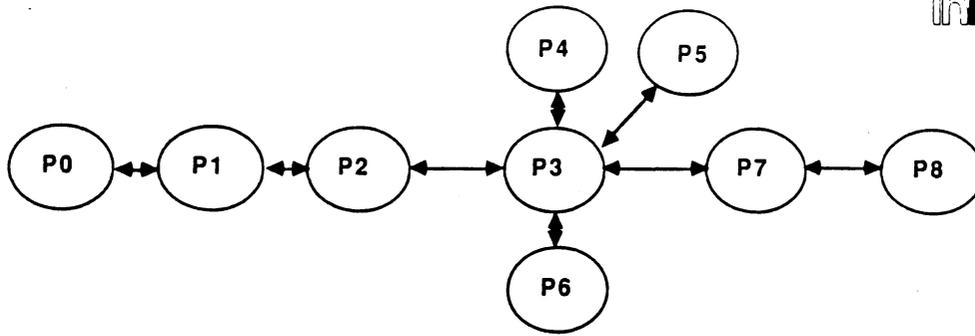
Computation and Communication run in parallel

Multiprocessing

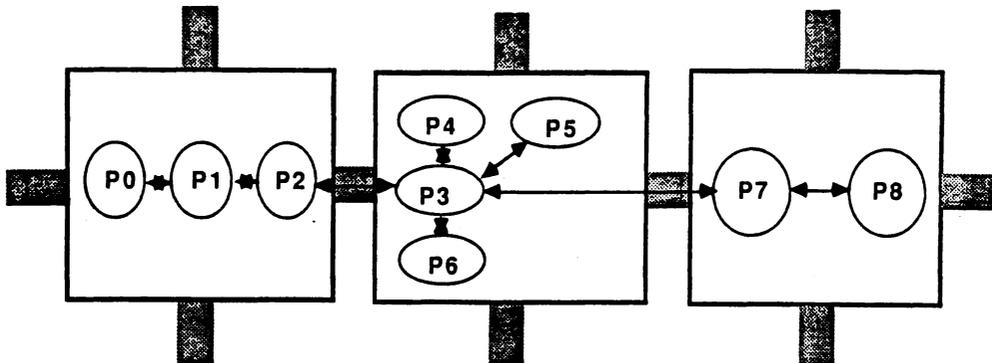


Concurrent Processes

- Run simultaneously
- Asynchronous
- Completely Independent
- Local Data Storage
- No shared variables
- Data Communicated via channels



Could be Mapped as :



The Transputer

Unique Architecture

Generic Transputer

Fast CPU - best of RISC and CISC !

Fast On-Board Memory

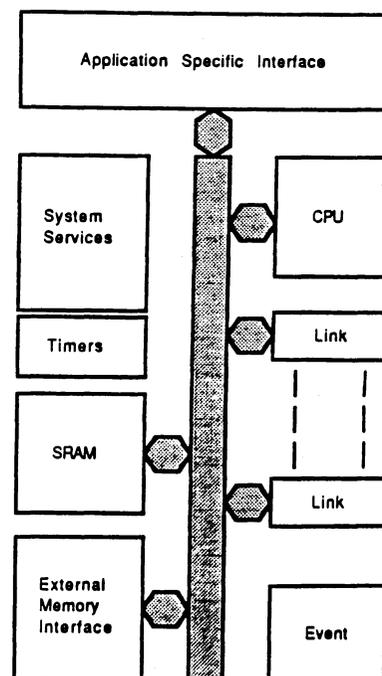
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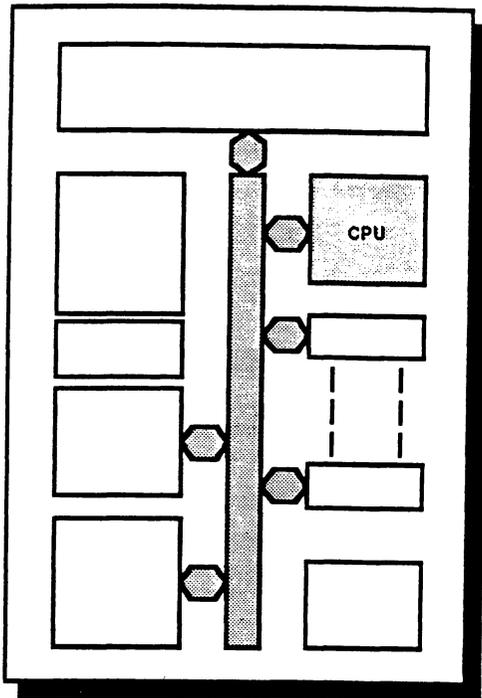
Virtual Timers

Minimum External Support circuitry

Simple System Engineering



Fast CPU



32 bit processor.
30 MIPS peak performance.

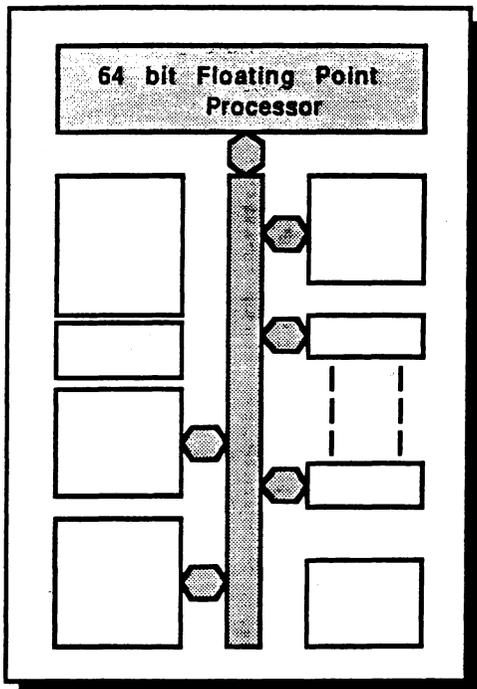
16 byte sized direct functions.
145 microcoded instructions.

Processor initiates link transfers
and FPU operations.

Sub microsecond process switch.
Instruction prefetch.

The best of RISC and CISC architectures !

Floating Point Unit



64 bit on-chip FPU

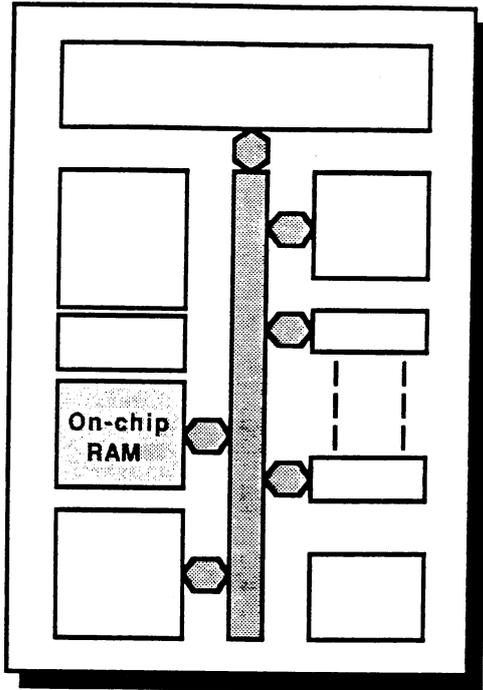
ANSI-IEEE 754-1985 representation.

Sustained 2.25 MFLOPS (30 MHz).

Overlaps with integer operations.

6.9M Whetstones/s
(single length @ 30 MHz)

On-Chip RAM



2 or 4 Kbytes of on-chip RAM.

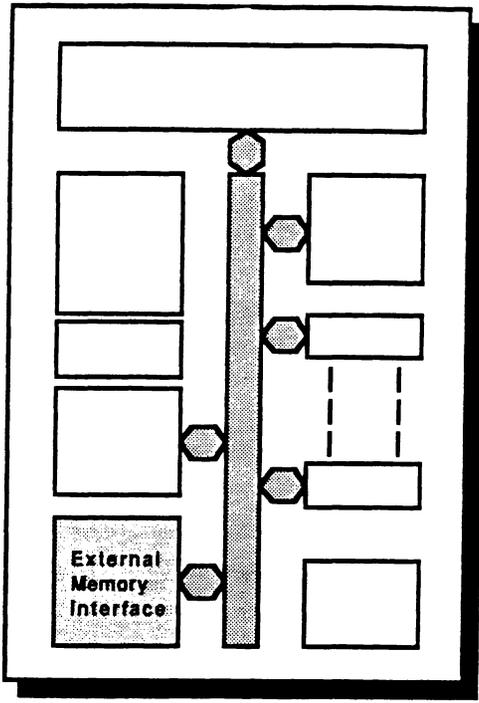
Single-cycle word access.

120 MBytes/sec bandwidth (30MHz).

Forms base of linear address space.

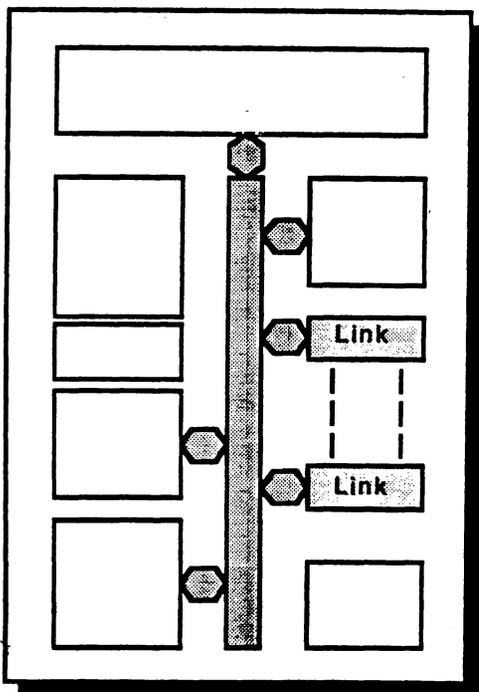


External Memory Interface



- Programmable Memory Controller.
- 32-bit multiplexed address/data bus or 32-bit non multiplexed address and data buses.
- Programmable timing and strobes.
- Configurable refresh.
- Support for mixed memory systems.
- Support for external DRAM
- 4 Gbyte address space - 32 bit parts
- 64 Kbyte address space - 16 bit parts

Serial Links

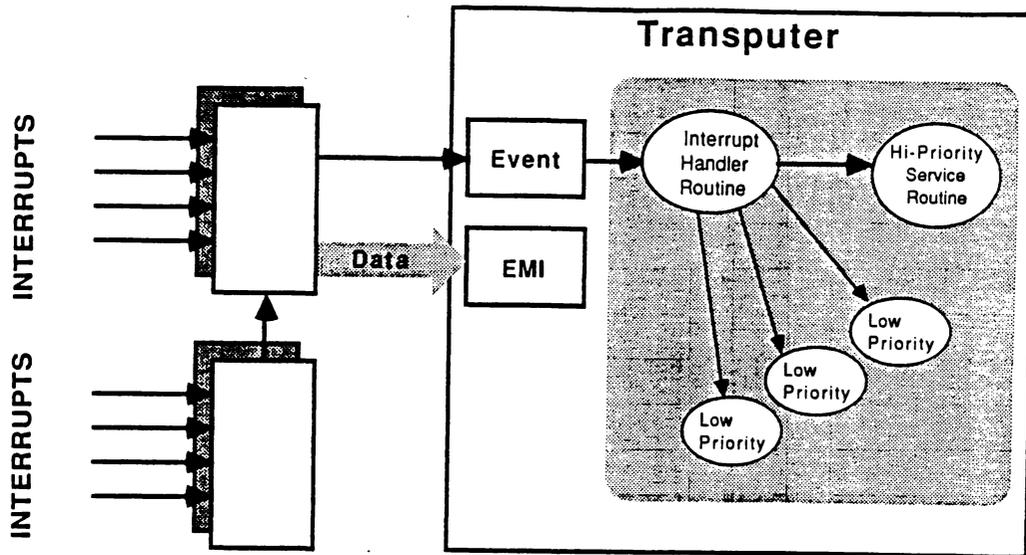


- Bi-directional asynchronous communications.
- Automatic acknowledgements per byte.
- 1.7 Mbytes/s uni-directional data transfer,
- 2.3 Mbytes/s bi-directional data transfer.
(For 1 link @ 20 Mbits)
- All link transfers and computation can overlap.
- Processor can bootstrap from any link.

Interrupts / Events

- Unique architecture simplifies Interrupt handling
- Simple 2 levels of priority (high and low)
- Very fast Interrupt response time - sub microsecond
- Incoming Interrupt is assigned to a process queue

Interrupt Handling



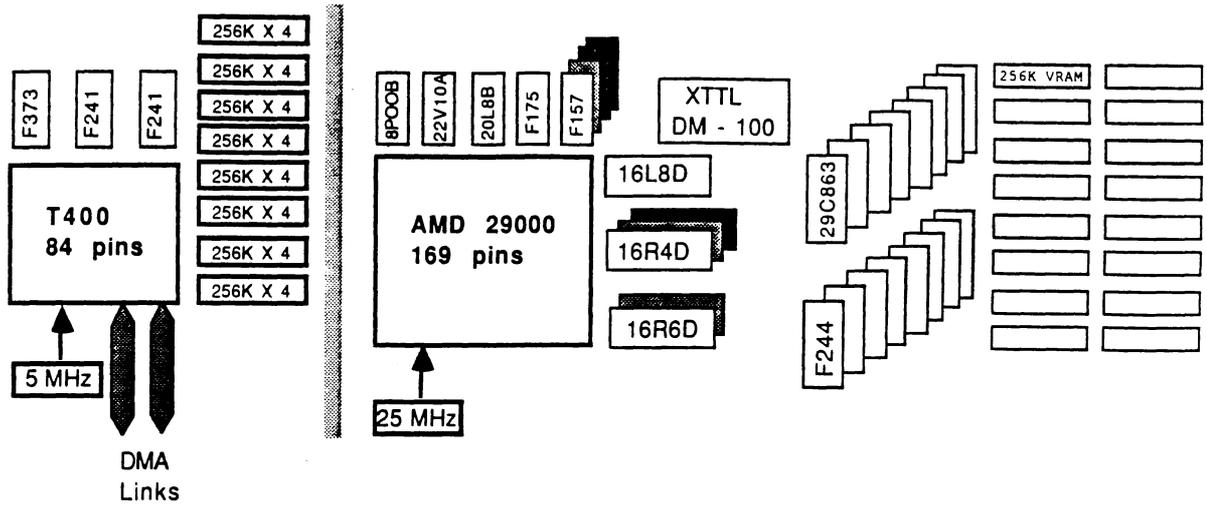
Interrupt Handler
eg. Intel 8259A

Interrupt Handler Routine assigns
priority to incoming interrupts

Low System Cost

- Low Pin Count 84/100 pin
- Single 5 MHz Clock input.
- Low Power Consumption - under 1 Watt
- On chip EMI - minimises external glue logic
- Two timers
- Interrupt Pin

T400 System Cost Comparison



10 MIPS, 1 Mbyte, 4.7 Mbyte/sec I/O
 12 Components
 Power < 5 Watts
 System Cost ratio - 1

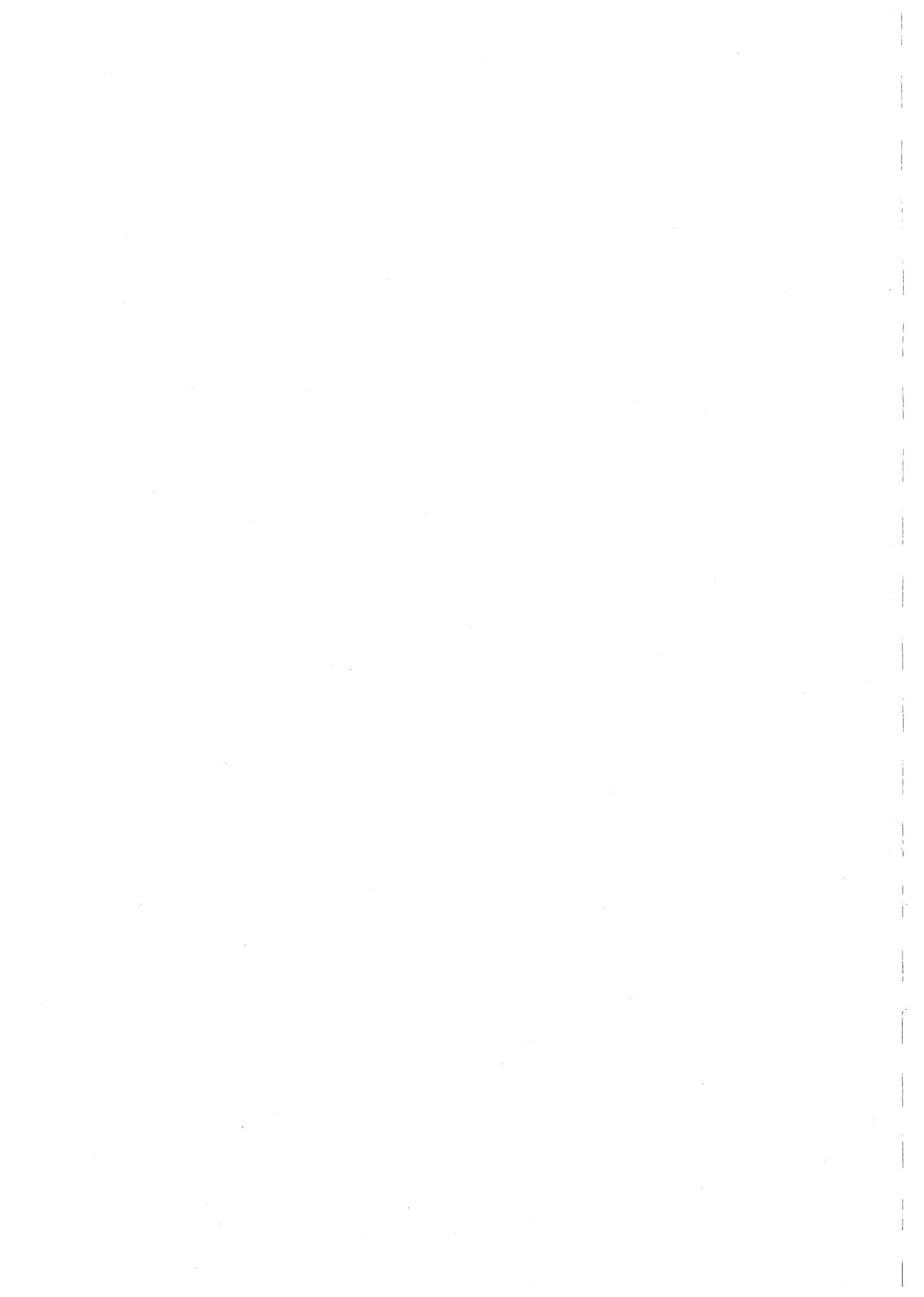
11.5 MIPS, 512KByte VRAM, NO I/O
 48 Components
 Power > 25 Watts
 System Cost Ratio - 5

Source: AMD - AMD 29000 Memory Design H/book



TUA A 011



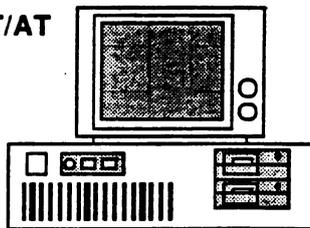


Transputer

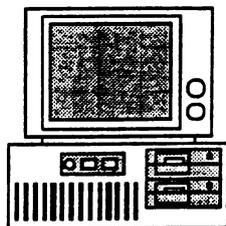
Development Made Simple

INMOS Development Hosts

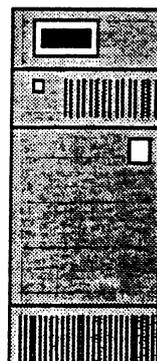
IBM XT/AT
PS2



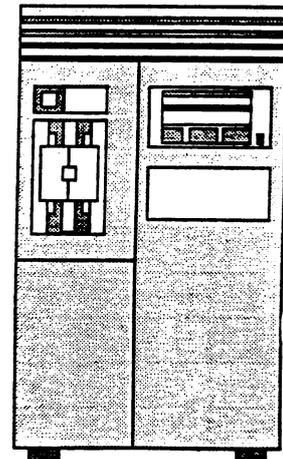
NEC
PC



Sun 3
Sun 4
Sun 386i



MicroVAX

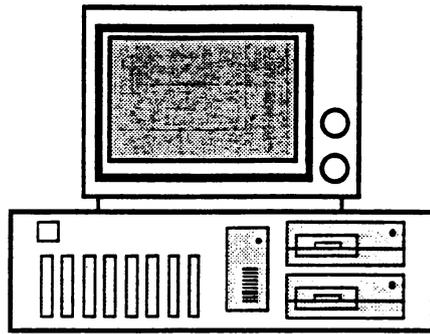


PC Development Made Simple



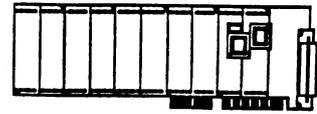
Software

C, Fortran
Pascal Ada
and occam



Host System

eg IBM PC, NEC PC,



Transputer Add-in Board

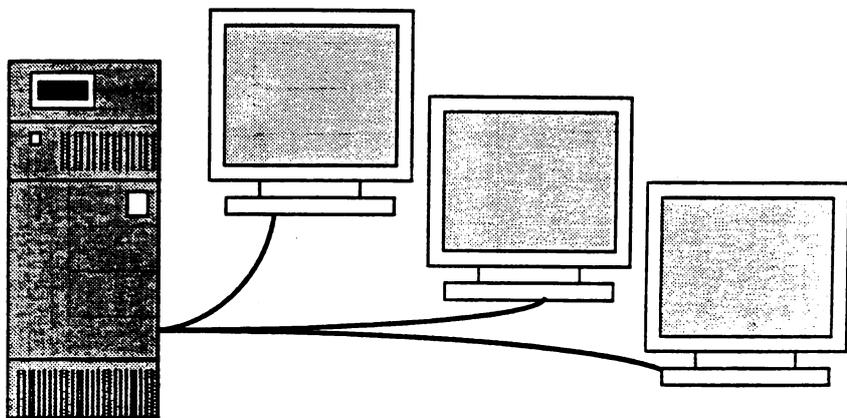
- * INMOS supports all common languages + Parallel Processing
- Customer can use existing software

SUN Development Made Simple



Software

C, Fortran
Ada & occam



Sun 3 workstation
VME motherboard
IMS BO14/BO16

Software Product Range

	SUN 3	SUN 4	VAX	IBM PS2/PC XT 386 i	NEC
occam Toolset	D505	D405	D605	D705	D705
C Compiler	D511		D611	D711	D711
C Toolset	D5214	D4214	D6214	D7214	D7214
Fortran	D513	D413	D613	D713	D713
Pascal				D712	D712

Transputer Toolsets

- Tools invoked from O/S command line (PC, SUN, VAX)
- Supports multi-user / multi-language development
- Interactive symbolic debugging (with Breakpoints)
- Post Mortem symbolic debugging
- Simulator
- Support for assembly language inserts
- Support for EPROM programming

INMOS Parallel Compilers

Compilers for occam, C and FORTRAN.

Validated - eg C Plum Hall suites.

Library support for parallelism

Optimizations - eg workspace allocation, dead code, instruction scheduling, constant folding.

Full ANSI C

Faster compilation and execution

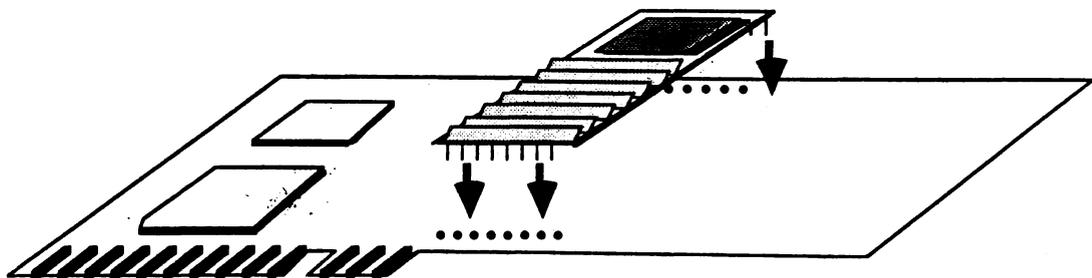
occam

- Designed to reflect transputer architecture.
- occam model consists of parallel processes communicating through channels.
- Channels allow data transfer between processes.
- Each process can be comprised of a set of processes.
- Other languages can be integrated by simply making them appear to be occam processes

INMOS Parallel Fortran

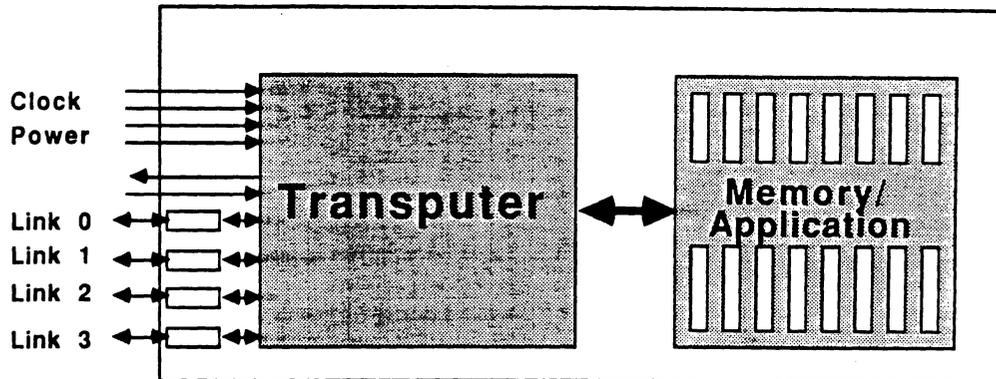
- Implements Fortran77, ANSI Std X3.9-1978 .
- Supports concurrent tasks.
- Ability to allocate stack in on-chip RAM.
- Available for SUN, VAX and PC.
- Configurers provided for multi-transputer development.
- Can be used standalone or with Toolset for mixed language support.

Mothercards



- IBM PC XT/AT
- VME
- PS2
- Double Eurocard
- NEC PC
- Third Party Products support other Hosts

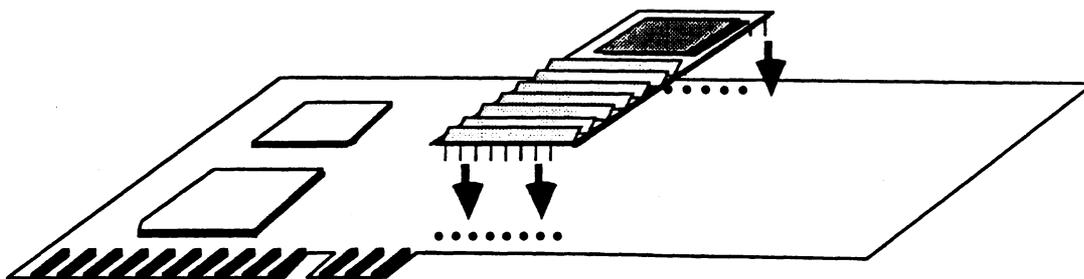
Unique Modular Hardware



A Transputer Module (TRAM)

- * TRAMs can be used to build prototype systems
- * INMOS/Third Party - Wide range of products

Transputer Introduction Kits



Includes :

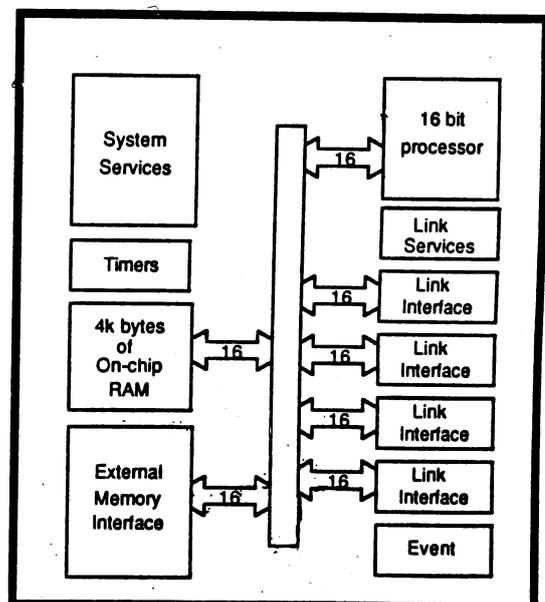
- IMS B008 IBM Motherboard
- IMS B404 T800 TRAM with 2 Mbytes DRAM
- Choice of Development Software

The Transputer

Products

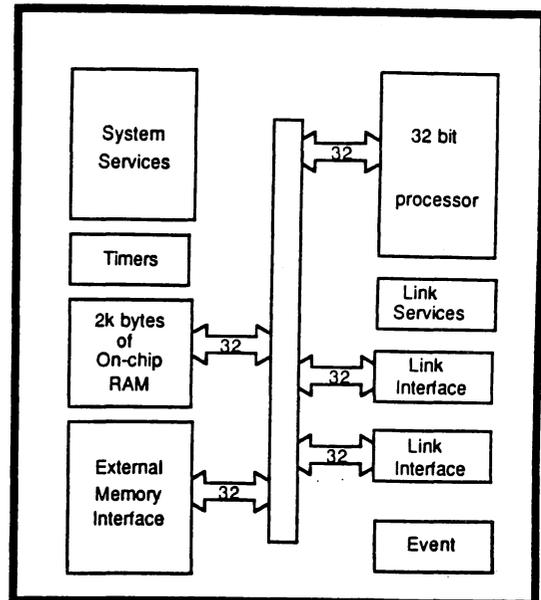
IMST225 transputer

- 16 bit architecture
- 30 MIPS (peak)
- 630 ns interrupt response
- 4 Kbytes on-chip SRAM
- 4 high speed serial links (5/10/20 Mbits/sec)
- 20, 25 and 30 MHz
- 68 pin PLCC, PGA and 100 PQFP packages



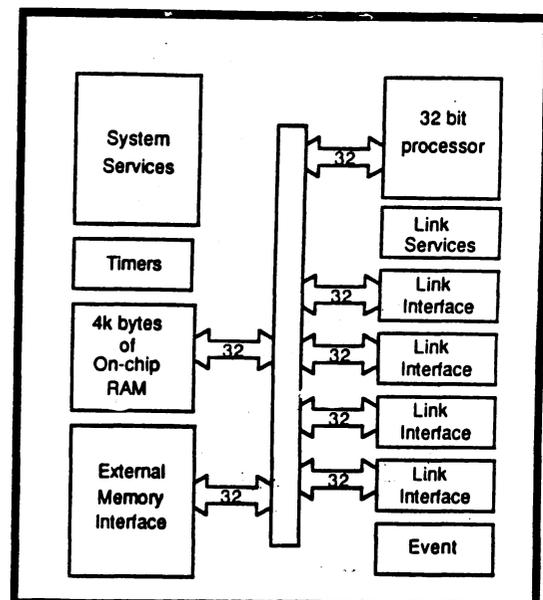
IMST400 - Low cost transputer - \$2/MIPS

- 32 bit architecture
- 20 MIPS (peak) 10 MIPS (sustained)
- 950 ns interrupt response
- 2 Kbytes on-chip SRAM
- 2 high speed serial links (5/10/20 Mbits/sec)
- 20 MHz single speed option
- 84 pin PGA, PLCC and 100 pin QFP



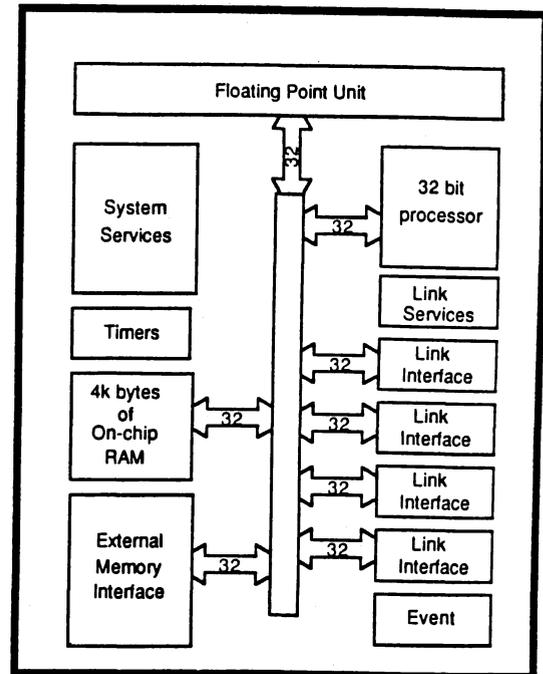
IMST425 transputer

- 32 bit architecture
- 30 MIPS (peak)
- 630 ns interrupt response
- 4 Kbytes on-chip SRAM
- 4 high speed serial links (5/10/20 Mbits/sec)
- 20 , 25 and 30 MHz
- 84 pin PLCC , PGA and 100 PQFP packages



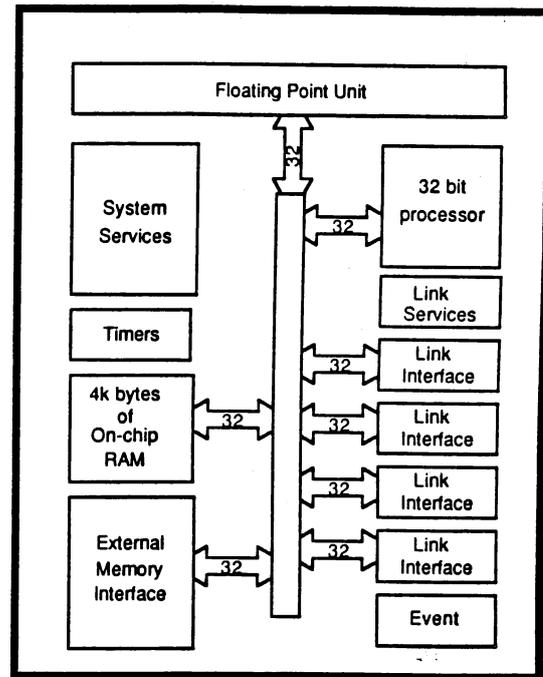
IMST805 transputer

- 32 bit architecture
- 30 MIPS (peak)
- On-chip IEEE 754 FPU
- 4.3 Mflops (peak)
- 630 ns interrupt response
- 4 Kbytes on-chip SRAM
- 4 high speed serial links (5/10/20 Mbits/sec)
- 20 , 25 and 30 MHz
- 84 pin PGA, PLCC and 100 PQFP packages



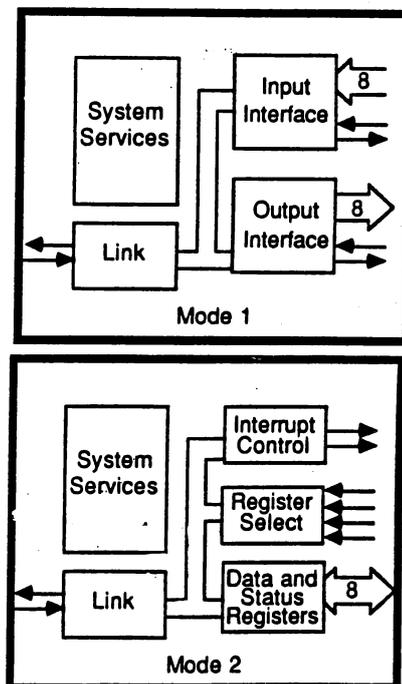
IMST801 transputer

- 32 bit architecture
- 30 MIPS (peak)
- On-chip IEEE 754 FPU
- 4.3 Mflops (peak)
- 630 ns interrupt response
- De-multiplexed address and data bus
- 60 Mbytes/sec data rate to external memory
- 4 Kbytes on-chip SRAM
- 4 high speed serial links (5/10/20 Mbits/sec)
- 20 , 25 and 30 MHz
- 100 pin PGA package.



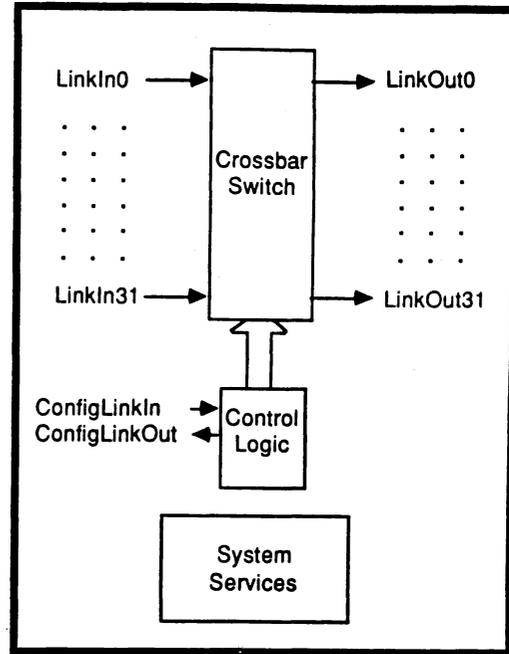
IMS C011 link adaptor

- Standard INMOS link protocol
- 5,10 or 20 Mbits/sec operating speed
- Communicates with INMOS transputers
- Converts between serial link and parallel bus.
- Mode 1: 8-bit peripheral interface.
- Mode 2: 8-bit bus interface.



IMS C004 programmable link switch

- Standard INMOS serial links
- 32 way crossbar switch
- Cascadable
- 10 or 20 Mbits/sec
- 84 pin PGA package



16 Bit Transputer Family

Family	Part No.	Serial Links	Speed (MHz)	On Chip SRAM	Package
T2 16 Bit CPU	T222-17S	4	17.5	4k	68 PGA/PLCC
	T222-20S	4	20.0	4k	68 PGA/PLCC
	T225-17S	4	17.5	4k	68 PGA/PLCC
	T225-20S	4	20.0	4k	& 100 PQFP
	T225-25S	4	25.0	4k	68 PGA
	T225-30S	4	30.0	4k	68 PGA

All parts have 64k byte Non -Multiplexed 2 Cycle External Memory Interface and 2 on-chip timers.

Use T225 for new designs

32 Bit Transputer Family

Family	Part No.	Serial Links	Speed (MHz)	On Chip SRAM	Package
T4 32 Bit CPU	T400-20S	2	20.0	2k	84 PGA/PLCC & 100 PQFP
	T425-17S	4	17.5	4k	84 PGA/PLCC
	T425-20S	4	20.0	4k	& 100 PQFP
	T425-25S	4	25.0	4k	
	T425-30S	4	30.0	4k	84 PGA

All parts have 4G byte Multiplexed External Memory Interface and 2 on-chip timers.

32 Bit Transputer Family with Floating Point Unit

Family	Part No.	Serial Links	Speed (MHz)	On Chip SRAM	Package
T8 32 Bit CPU + on chip FPU	T801-20S	4	20.0	4k	100 PGA
	T801-25S	4	25.0	4k	
	T801-30S	4	30.0	4k	
	T805-17S	4	17.5	4k	84 PGA/PLCC & 100 PQFP
	T805-20S	4	20.0	4k	
	T805-25S	4	25.0	4k	84 PGA
	T805-30S	4	30.0	4k	

T805 has 4G byte Multiplexed External Memory Bus
and T801 has 4G Non-Multiplexed Bus. All parts have 2 on-chip timers.

Transputer Family

Communications Peripherals

Part Number	Speed Mbits/sec	Package	Comments
IMS C004	5/10/20	84 PGA/QFP	32 way crossbar switch
IMS C011-20S	5/10/20	28 DIP 28 SOJ	Link to parallel interface. Mode1: 8 bit parallel interface. Mode2: bidirectional 8 bit bus.
IMSC012-20S	5/10/20	24 DIP	C011 mode2 only

Transputer Family

Military Qualified MIL STD 883C

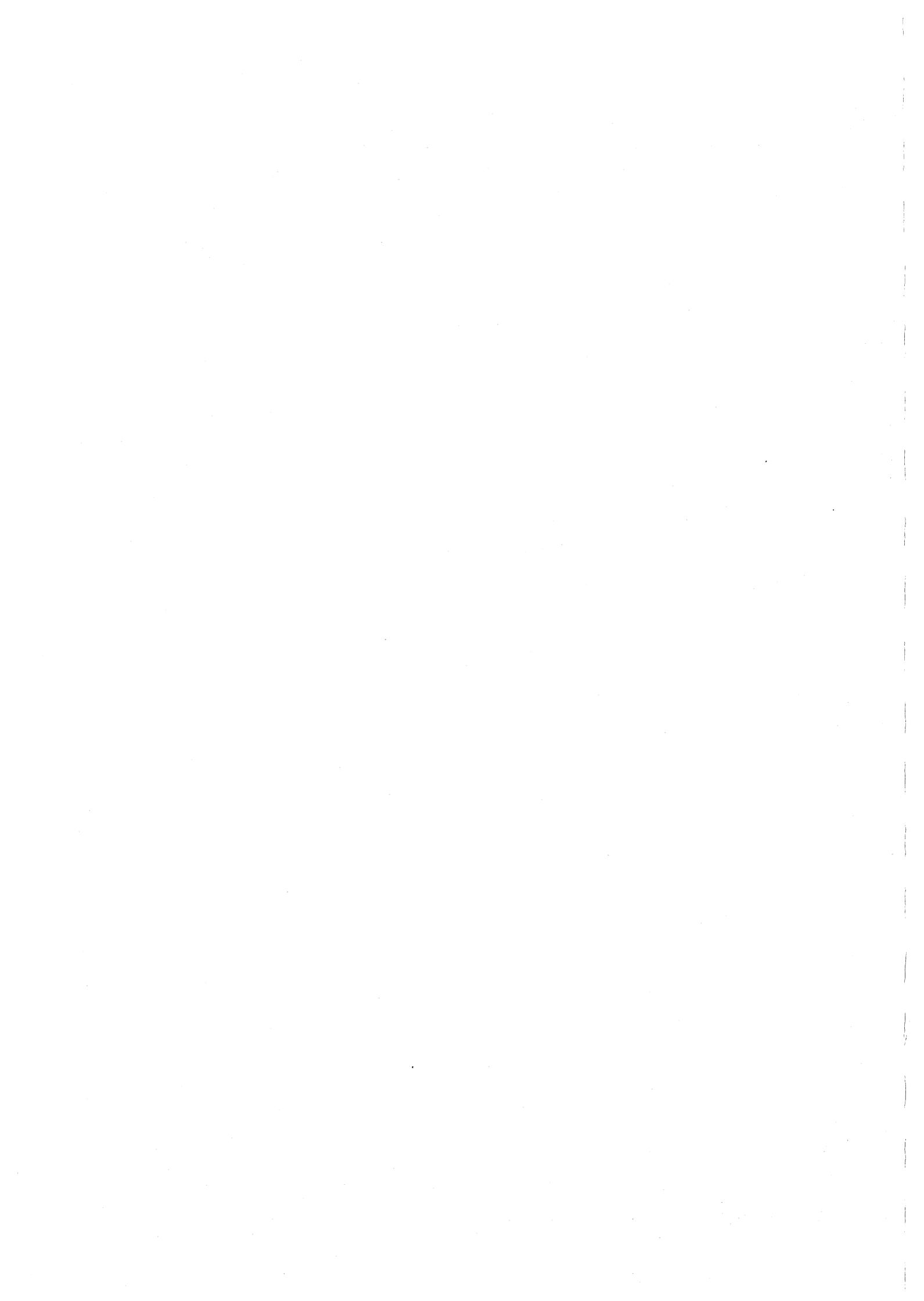
Family	Part Number	Speed (MHz)	SRAM	Package
T2 16 Bit CPU	T222-17M	17	4k	68 PGA
T4 32 Bit CPU	T425-17M	17	4k	84 PGA
T8 32 Bit CPU+FPU	T800-17M	17	4k	84 PGA/QCP
Peripherals	C011-20M	10/20		28 Cer. DIP
	C004-20M	10/20		84 PGA/QCP

Transputer Family

Military Qualified MIL STD 883C

Family	Part Number	Speed (MHz)	SRAM	Package
T2 16 Bit CPU	T225-20M	20	4k	68 PGA / 100 CQFP
T4 32 Bit CPU	T425-20M	20	4k	84 PGA / 100 CQFP
T8 32 Bit CPU+FPU	T805-20M	20	4k	84 PGA / 100 CQFP
	T801-20M	20	4k	100 PGA
Peripherals	C011-20M	10/20		28 DIP / LCCC
	C004-20M	10/20		84 PGA / 100 PQFP

Planned Products



Transputer

Who's Using it ?

Transputer Target Applications

Office Automation

Page Printers
X-Windows
Terminals
Fax Machines
Disk Arrays

PC & Workstations

Application
Accelerators
Graphics/Display
Supercomputers

Telecoms

Network
Management
Datacomms
Telephone
Exchanges
Satellites

Control

Radar/Sonar
Missiles + Smart
Weapons
Avionics
Simulators

Robotics
Machine Control
Factory Automation
Medical Imaging

Military

Transputer Applications

Kobe Steel

- Location: Japan
- Application: Graphics add-in card for NEC PC.
- Description: T800 based graphics card for the NEC PC using "hoops" software. Performance of the system can be increased by adding additional cards.
- The transputer was chosen as the processor because of the need for scalable performance.

Transputer Applications

Toyo Communications

- Location: Japan
- Application: Artificial Intelligence Workstation
- Description: System is a standalone workstation running under a version of Unix. Minimum configuration uses 4 IMST414 with the option to upgrade with more transputers for improved performance.
- Toyo Comm has published several papers in Japan on their work in Artificial Intelligence using transputers.

Transputer Applications

Pixar

- Location: California, US
- Application: Transputer accelerator for SUN's, PC's and SGI workstations for generation of high quality images using the "Renderman" scene description interface.
- Description:
 - 1- VME Raster Imaging Processor using 16 T800's per card.
 - 2- PC Raster Imaging Processor using 2 T800's per card.
- Development Environment: SUN workstations and C compiler.
- " The transputer was used for its ease of design and cost/performance"

Transputer Applications

Parsytec

- Location: Aachen, Germany
- Application: Modular cluster-oriented computer system.
- Description: Each module comprises 64 x IMST800, 6 x IMST425 and 6 x IMST222. Each system can be expanded by adding additional modules. Offers Helios operating system and Megatool (a port of the TDS).
- Development Environment: MEGATOOL
- Product Name: Supercluster
- "Transputer and occam offer the only meaningful solution for parallel processing." (Dr. Peise, Parsytec)

Transputer Applications

Yasakawa Electric Mfg

- Location: Japan
- Application: Expert System
- Description: A high performance real-time system to be applied to diagnostic/control of PLC's, robots and numerical controllers. Uses 17 IMST800 running an OPS5 structured language.
- Product Name: RTPS (Real Time Production System)

Transputer Applications

CSS

- Location: California, US
- Application: Laser Printer Controller
- Description: A single T414 can do emulation of existing printer cntl codes and print at about 55 pages per minute. By adding extra transputers the board will easily handle next generation colour laser printers
- Development Environment: TDS
- "Occam is a fast and efficient language allowing me to do all that low level control quite easily. My biggest surprise is that when I translate C code into occam that it is now smaller and faster."

Transputer Applications Columbus Positioning Ltd.

- Location : UK
- Application : Global Positioning By Satellite (GPS)
- Description : A portable hand held unit capable of giving a position fix within 10 seconds to an accuracy of 10 m. The unit uses a single T800 transputer.
- Product Name : Gypsy

Transputer Applications General Dynamics

- Location: California, US
- Application: Image enhancement and recognition.
- Description: System includes 5 IMST800's and 4 IMSA100's for a target recognition and battle management system. Scalable performance improvement is important for future enhancements.
- Development Environment: TDS
- "Occam is such an elegant way of doing this. With a 2-5us message overhead, why should I use an Operating System with its excess luggage giving us 150us overhead per message."

Transputer Applications

Cogent Research

- Location: Oregon, US
- Application: Modular desk-top parallel-processing supercomputer.
- Description: Basic system has 2 T800's. Can add up to 334 T800's. Uses Linda, a parallel processing software environment.
- Product Name: XTM
- "Compute power previously found only in vector processors is now available in a general purpose computer, where it can be harnessed for simulation, modelling, graphics and inferencing, as well as scientific computation." (Affordable Supercomputing through Parallel Processing, 1988).

Transputer Applications

KDD

- Location: Japan
- Application: Video Telephone
- Description: Uses up to 20 IMST425's for transmission of still pictures on telephone lines.
- Required the performance of parallel processing

Transputer Applications

Merino Wool Harvesting

- Location: Adelaide, Australia
- Application: Portable robotic sheep shearer
- Description: Uses multiple T800's to get the performance needed where system cost and size were important. Could not get the same scalable performance from traditional microprocessors.
- Using occam to port the application to multiple T800's

Transputer Applications

NASA

- Location: Johnson Space Center, US
- Application: Robotics
- Description: The "EVA-Retriever" is a self-propelled vehicle for use with the Space Station and Space Shuttle for retrieval of objects in space. T800's are used as the main central processors with T2's used as intelligent peripheral controllers. The design required the processing power and scalability of the transputer to handle the various tasks needed (i.e. pattern recognition, reasoning, perception, world modelling etc.) where space and power were limited.
- Product Name: EVA-Retriever

Transputer Applications

Marconi Defence Systems

- Location: Bracknell, UK
- Application: Radar Defence System
- Description : Scalable radar system comprised of multiple Transputer nodes each using 50 T222's for data processing. Range of system sizes up to large 5,000 transputer system.
- " The transputer - the most cost effective array technology."

iq systems

iq Systems Charter

To provide an extensive range of innovative modular hardware and software products to meet the high quality standards and service requirements of the OEM and system developer.

iq systems

Innovation and Quality



Innovation

Flexible Modular Architecture
for multiprocessor systems.

Quality

Mature range of industry standard
software tools.

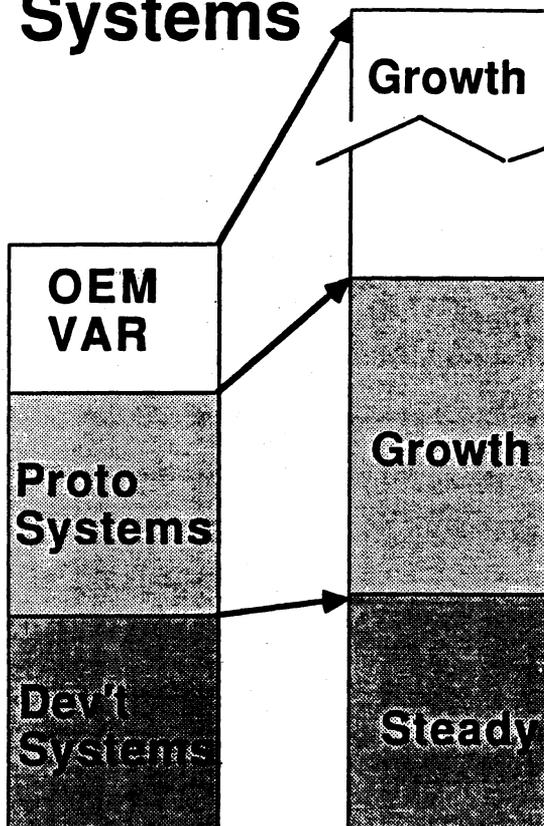
Rigorous design, production and
QA standards.

Technical Support Worldwide



IQS A 003

iq Systems



OEM and system integrator
business. Adds value with
s/w and system solutions.

Prototyping business for
board manufacturers.
Unique concept.
Expanding quickly.

Core business to support
silicon design-ins.



IQS A 004

iq Systems

Benefits for 3 Market Segments

1. Transputer Application Development

To support board level designers build transputer based systems.

2. Transputer System Prototyping

To allow board level designers to build proof of concept and pre-production systems.

3. End System Integration

To offer a range of board level products to system integrators and Value Added Resellers.

1 Transputer Application Development

Comprehensive range of mature tools for single and multiprocessor projects

Available for PC, PS2, SUN and VAX hosts

Common tools for both 16 and 32-bit processors

Industry standard languages C, Fortran, Pascal and occam

Extensive range of 3rd Party Development tools

Backed up by a worldwide network of technical support centres

2 Transputer System Prototyping

iq Systems minimises development costs and accelerates projects to market by :

- Using common H/W for design and prototyping
- Providing an extensive range of complimentary products for a variety of applications
- Supercomponent concept fully supported with software provides plug in and run capability

Early prototyping means early system software development giving faster time to market !

3. End System Integration

- Most efficient modular processing architecture for flexible end systems
- Fully compatible with industry standard buses eg. VME, MCA etc
- Increased return on investment through extended S/W life cycles
- One system design will meet variety of end product performance and configurations
- Common TRAM components across variety of systems performances and hosts, reducing inventory holding

iq Systems - Existing Customer Examples

Henson

Application

- Dental CAD System
- Supplied direct to Dentists

Company Profile

- 35 people (20 Engineers)
- System Integrator
- Buy 'off the shelf' Hardware
- S/W Experience in the End application

Why ?

- Interface to Standard Bus available
- Multi-processor Power (3 Transputers Used)