SGS-THOMSON MICROELECTRONICS

IMS C004

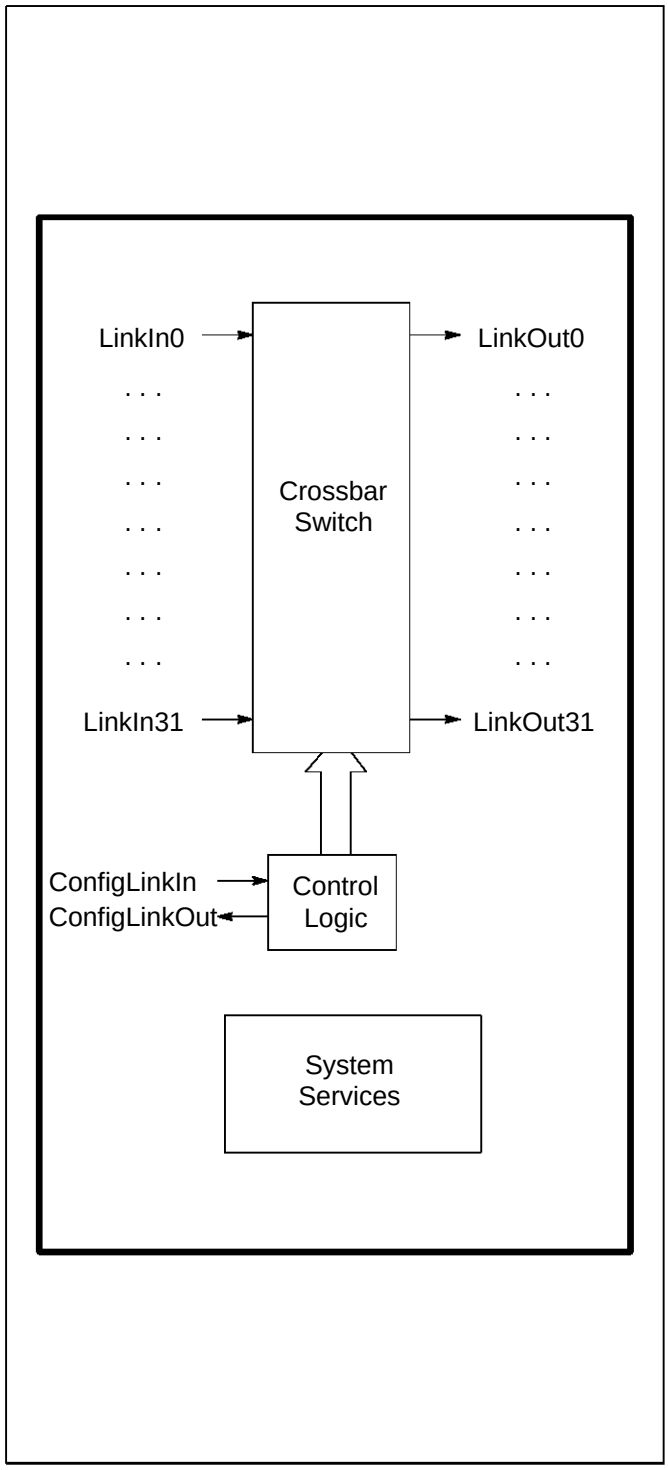
Programmable link switch

FEATURES

- Standard INMOS serial links
- 32 way crossbar switch
- Regenerates input signal
- Cascadable to any depth
- No loss of signal integrity
- 10 or 20 Mbits/sec operating speed
- Separate INMOS configuration link
- Single +5V 5% power supply
- TTL and CMOS compatibility
- 1W power dissipation
- Packaging 84 pin PGA

APPLICATIONS

- Programmable crossbar switch
- Component of larger switch
- Reconfigurable supercomputers
- Message routing system
- High speed multiprocessor systems
- Telecommunications
- Robotics
- Fault tolerant systems
- Additional links for transputers



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Contents

1 Introduction

The INMOS communication link is a high speed system interconnect which provides full duplex communication between transputers, according to the INMOS serial link protocol. The IMS C004 is a transparent programmable link switch designed to provide a full crossbar switch between 32 link inputs and 32 link outputs.

The IMS C004 will switch links running at either the standard speed of 10 Mbits/sec or at the higher speed of 20 Mbits/sec. It introduces, on average, only a 1.75 bit time delay on the signal. Link switches can be cascaded to any depth without loss of signal integrity and can be used to construct reconfigurable networks of arbitrary size. The switch is programmed via a separate serial link called the *configuration link*.

All products which use INMOS communication links, regardless of device type, support a standard communications frequency of 10 Mbits/sec; most products also support 20 Mbits/sec. Products of different type or performance can, therefore, be interconnected directly and future systems will be able to communicate directly with those of today.

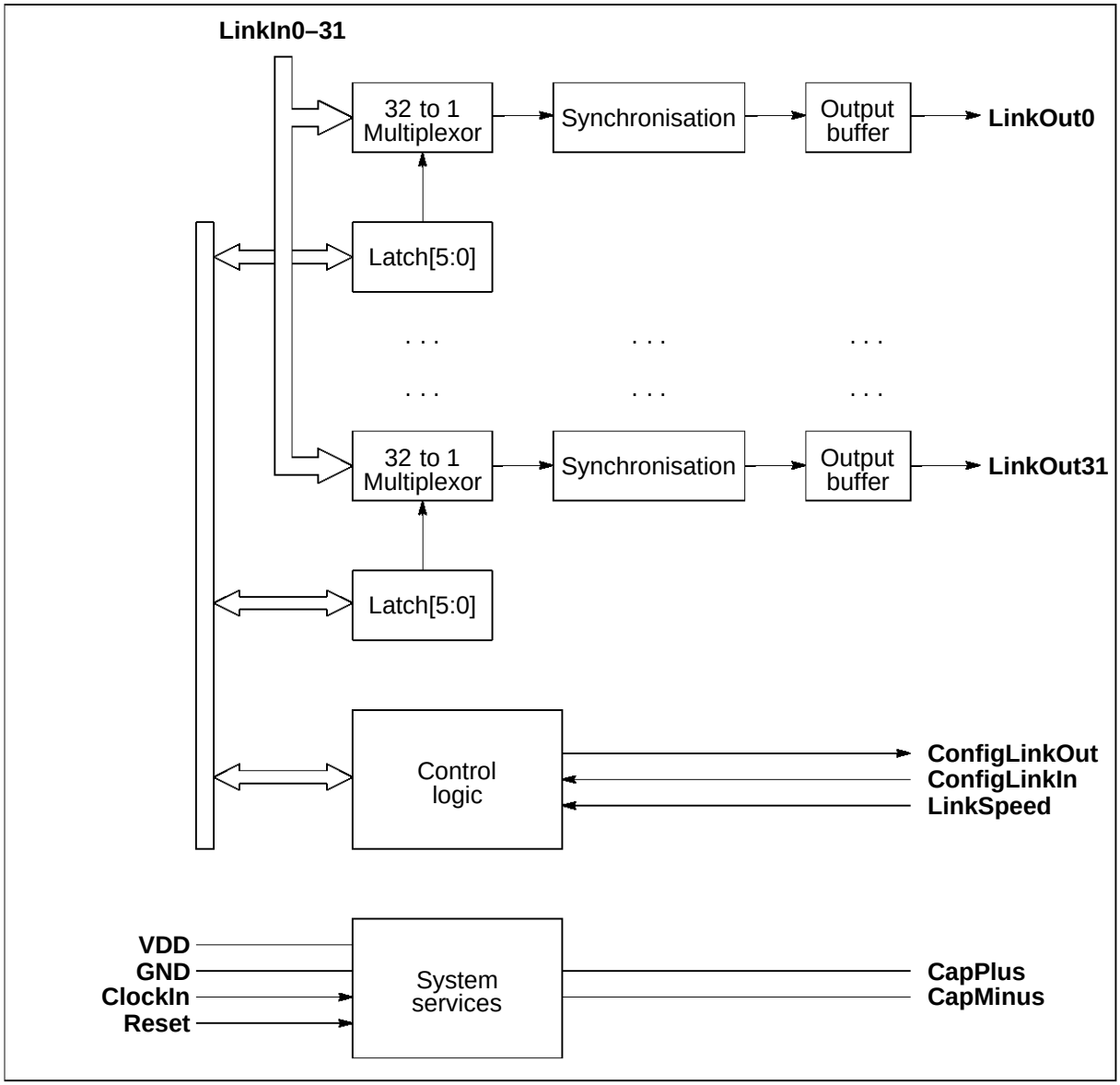


Figure 1.1 IMS C004 block diagram

2 Pin designations

Signal names are prefixed by **not** if they are active low, otherwise they are active high.
Pinout details are given on page 20.

Pin	In/Out	Function
VDD, GND		Power supply and return
CapPlus, CapMinus		External capacitor for internal clock power supply
ClockIn	in	Input clock
Reset	in	System reset
DoNotWire		Must not be wired

Figure 2.1 IMS C004 system services

Pin	In/Out	Function
ConfigLinkIn	in	INMOS configuration link input
ConfigLinkOut	out	INMOS configuration link output

Figure 2.2 IMS C004 configuration

Pin	In/Out	Function
LinkIn0-31	in	INMOS link inputs to the switch
LinkOut0-31	out	INMOS link outputs from the switch
LinkSpeed	in	Link speed selection

Figure 2.3 IMS C004 link

3 System services

System services include all the necessary logic to start up and maintain the IMS C004.

3.1 Power

Power is supplied to the device via the **VDD** and **GND** pins. Several of each are provided to minimise inductance within the package. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100 nF low inductance (e.g. ceramic) capacitor between VDD and GND. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

Input voltages must not exceed specification with respect to **VDD** and **GND**, even during power-up and power-down ramping, otherwise *latchup* can occur. CMOS devices can be permanently damaged by excessive periods of latchup.

3.2 CapPlus, CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1µF capacitor to be connected between **CapPlus** and **CapMinus.** A ceramic capacitor is preferred, with an impedance less than 3 Ohms between 100kHz and 10MHz. If a polarised capacitor is used the negative terminal should be connected to **CapMinus**. Total PCB track length should be less than 50 mm. The connections must not touch power supplies or other noise sources.

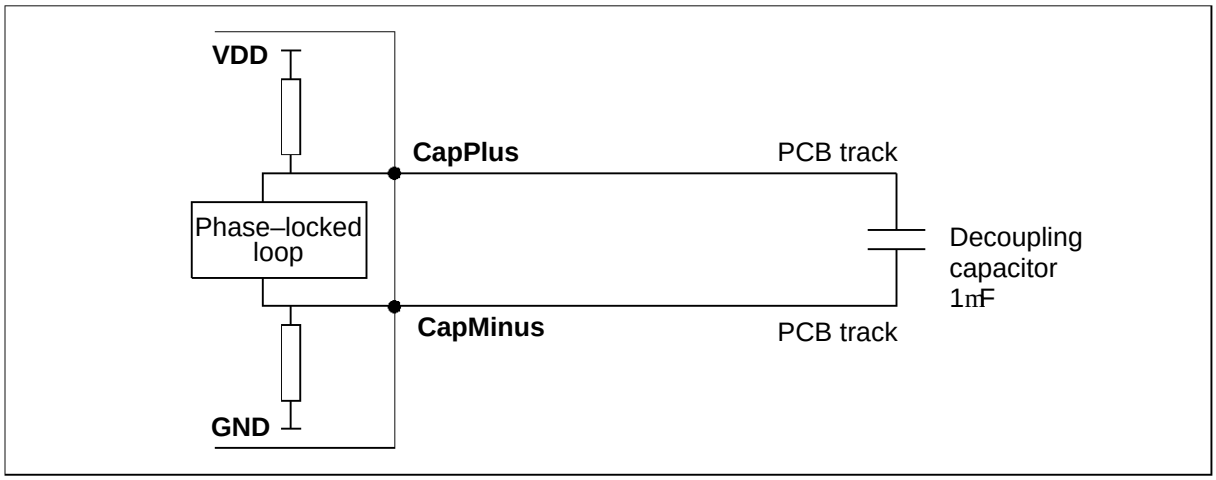


Figure 3.1 Recommended PLL decoupling

3.3 ClockIn

Transputer components use a standard clock frequency, supplied by the user on the **ClockIn** input. The nominal frequency of this clock for all transputer components is 5 MHz, regardless of device type, transputer word length or processor cycle time. High frequency internal clocks are derived from **ClockIn**, simplifying system design and avoiding problems of distributing high speed clocks externally.

A number of transputer devices may be connected to a common clock, or may have individual clocks providing each one meets the specified stability criteria. In a multi-clock system the relative phasing of **ClockIn** clocks is not important, due to the asynchronous nature of the links. Mark/space ratio is unimportant provided the specified limits of **ClockIn** pulse widths are met.

Oscillator stability is important. **ClockIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **ClockIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TDCLDCH	**ClockIn** pulse width low	40			ns	
TDCHDCL	**ClockIn** pulse width high	40			ns	
TDCLDCL	**ClockIn** period		200		ns	1,3
TDCerror	**ClockIn** timing error			0.5	ns	2
TDC1DC2	Difference in **ClockIn** for 2 linked devices			400	ppm	3
TDCr	**ClockIn** rise time			10	ns	4
TDCf	**ClockIn** fall time			8	ns	4

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their nominal times.

3 This value allows the use of 200ppm crystal oscillators for two devices connected together by a link.

4 Clock transitions must be monotonic within the range **VIH** to **VIL** (table 7.3).

Table 3.1 Input clock

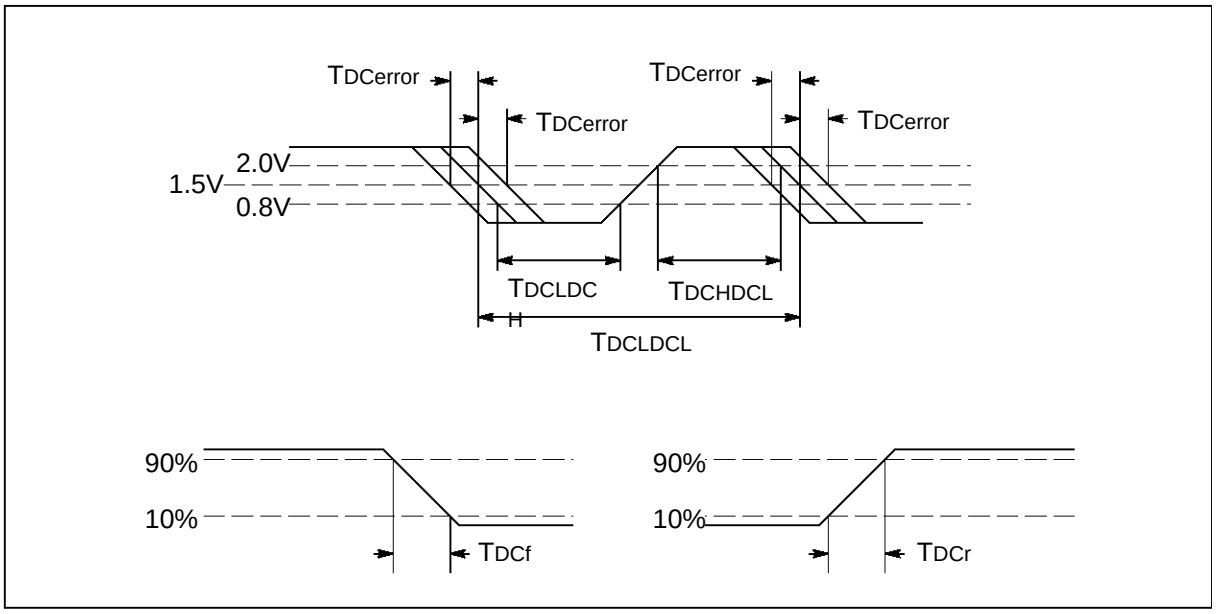


Figure 3.2 **ClockIn** timing

3.4 Reset

The **Reset** pin can go high with **VDD**, but must at no time exceed the maximum specified voltage for **VIH**. After **VDD** is valid **ClockIn** should be running for a minimum period **TDCVRL** before the end of **Reset**.

Reset initialises the IMS C004 to a state where all link outputs from the switch are disconnected and held low; the control link is then ready to receive a configuration message.

Symbol	Parameter	Min	Nom	Max	Unit	Notes
TPVRH	Power valid before Reset	10			ms	
TRHRL	Reset pulse width high	8			**ClockIn**	1
TDCVRL	ClockIn running before Reset end	10			ms	2

Notes

1 Full periods of **ClockIn TDCLDCL** required.

2 At power-on reset.

Table 3.2 Reset

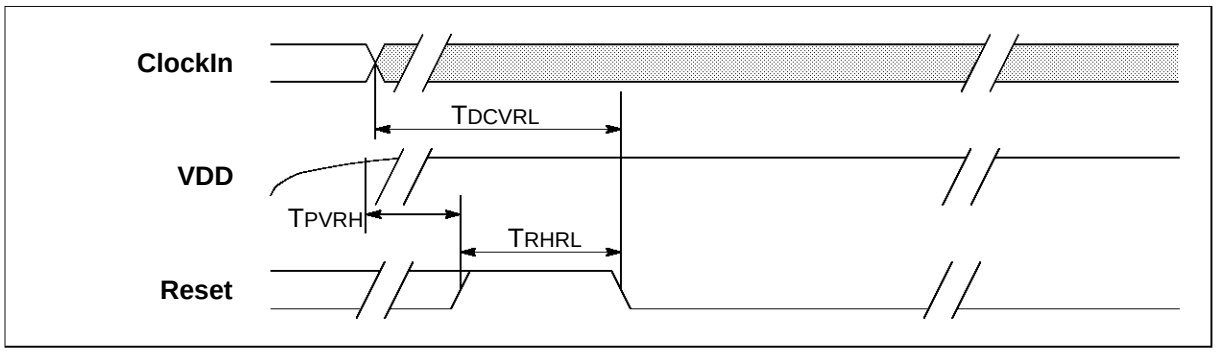


Figure 3.3 Reset timing

4 Links

INMOS bi-directional serial links provide synchronized communication between products and with the outside world. Each link comprises an input channel and output channel. A link between two devices is implemented by connecting a link interface on one to a link interface on the other device. Every byte of data sent on a link is acknowledged on the input of the same link, thus each signal line carries both data and control information.

A receiver can transmit an acknowledge as soon as it starts to receive a data byte. In this way the transmission of an acknowledge can be overlapped with receipt of a data byte to provide continuous transmission of data. This technique is fully compatible with all other transputer links.

The quiescent state of a link output is low. Each data byte is transmitted as a high start bit followed by a one bit followed by eight data bits followed by a low stop bit. The least significant bit of data is transmitted first. After transmitting a data byte the sender waits for the acknowledge, which consists of a high start bit followed by a zero bit. The acknowledge signifies hat the receiving link is able to receive another byte.

Links are TTL compatible and intended to be used in electrically quiet environments, between devices on a single printed circuit board or between two boards via a backplane. Direct connection may be made between devices separated by a distance of less than 300 millimetres. For longer distances a matched 100 ohm transmission line should be used with series matching resistors **RM**. When this is done the line delay should be less than 0.4 bit time to ensure that the reflection returns before the next data bit is sent.

Buffers may be used for very long transmissions. If so, their overall propagation delay should be stable within the skew tolerance of the link, although the absolute value of the delay is immaterial.

The IMS C004 links support the standard INMOS communication speed of 10Mbits/s. In addition they can be used at 20 Mbit/s. When the **LinkSpeed** pin is low, all links operate at the standard 10Mbit/s;when high they operate at 20Mbits/s.

A single IMS C004 inserted between two transputers which fully implement overlapped acknowledges will cause some reduction in data bandwidth, see table 4.2 and figure 4.7.

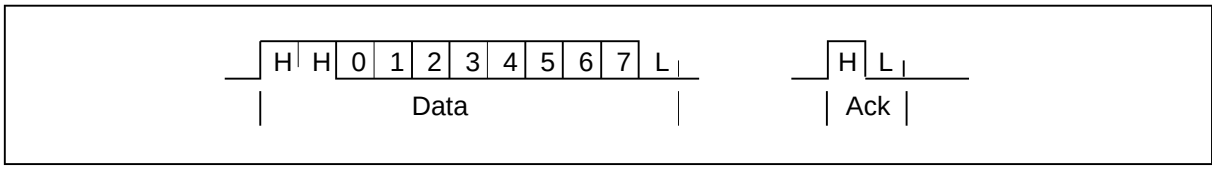


Figure 4.1 IMS C004 link data and acknowledge packets

Symbol	Parameter		Min	Nom	Max	Unit	Notes
T_{JQr}	LinkOut rise time				20	ns	
T_{JQf}	LinkOut fall time				10	ns	
T_{JDr}	LinkIn rise time				20	ns	
T_{JDf}	LinkIn fall time				20	ns	
T_{JQJD}	Buffered edge delay		0			ns	
T_{JBskew}	Variation in T_{JQJD}	20 Mbits/s			3	ns	1
		10 Mbits/s			10	ns	1
C_{LIZ}	LinkIn capacitance	@f=1MHz			7	pF	
C_{LL}	LinkOut load capacitance				50	pF	
R_M	Series resistor for 100Ω transmission line			56		Ω	

Notes

1 This is the variation in the total delay through buffers, transmission lines, differential receivers etc., caused by such things as short term variation in supply voltages and differences in delays for rising and falling edges.

Table 4.1 Link

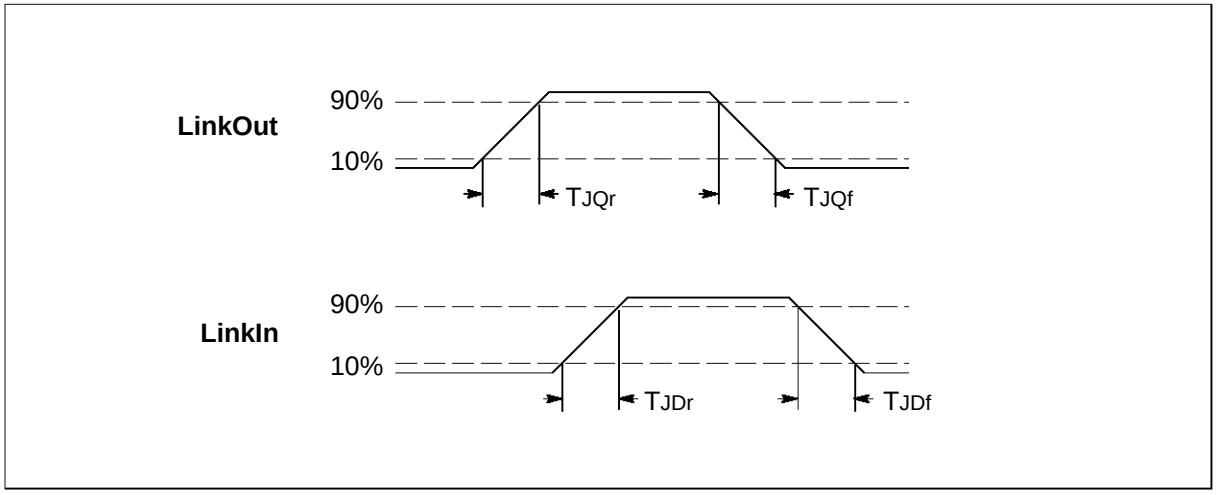


Figure 4.2 IMS C004 link timing

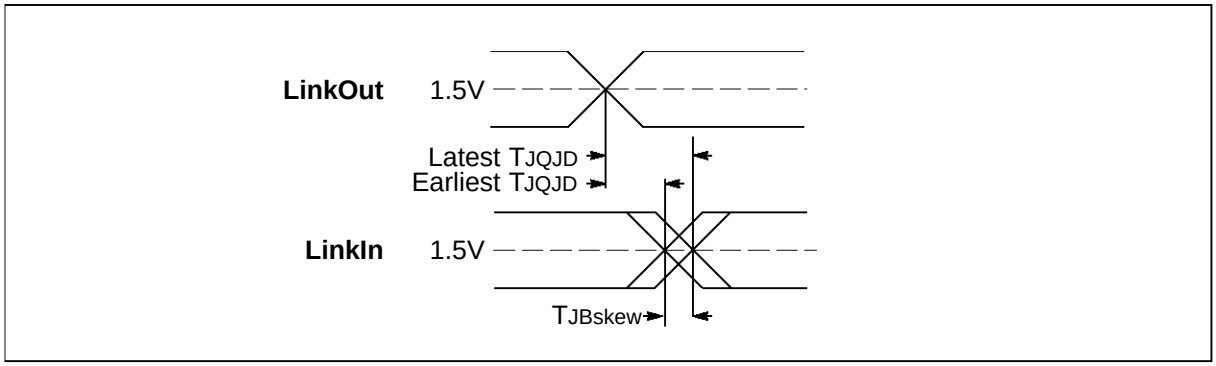


Figure 4.3 IMS C004 buffered link timing

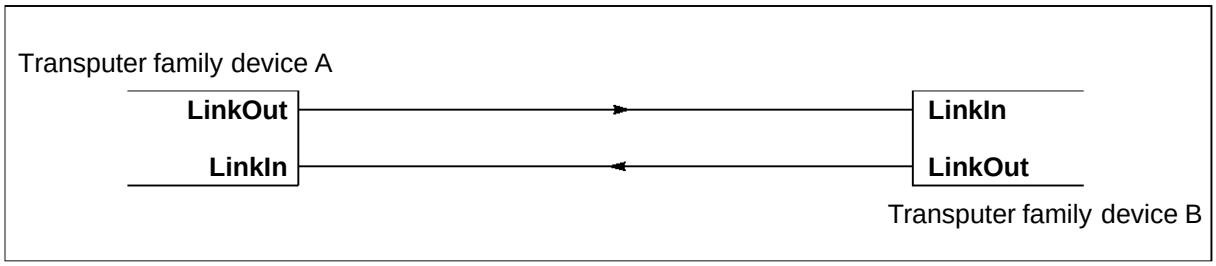


Figure 4.4 IMS C004 links directly connected

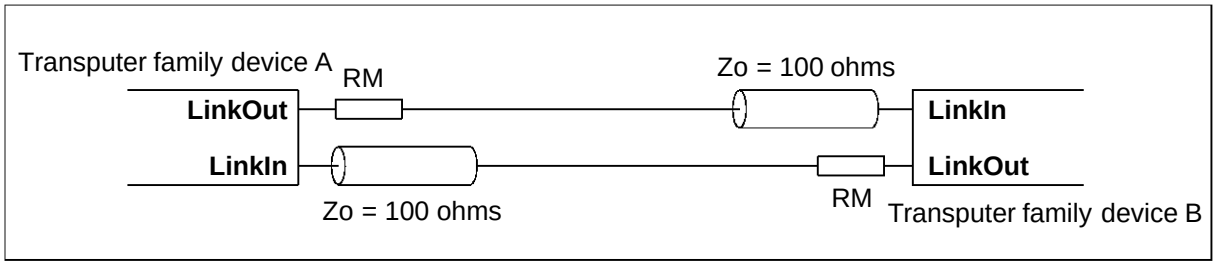


Figure 4.5 IMS C004 links connected by transmission line

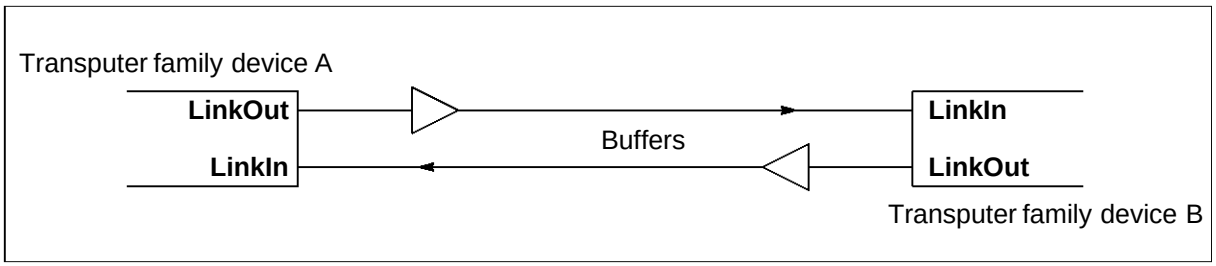
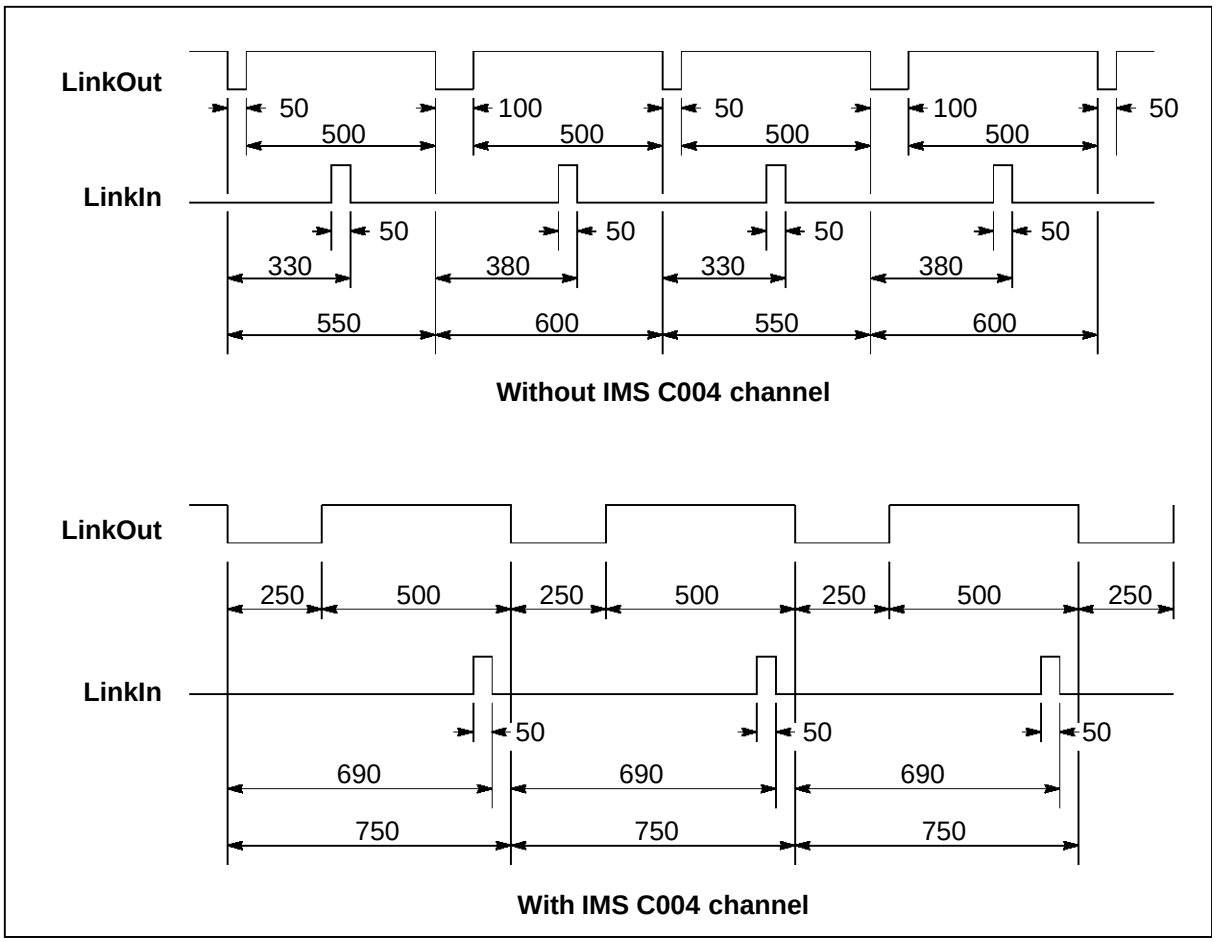


Figure 4.6 IMS C004 links connected by buffers

	Without C004	With C004	Degradation
Unidirectional	1.7	1.3	25%
Biderectional	2.3	2.1	10%

Table 4.2 T800 links data transfer rate at 20Mbit/s



Notes

1 All values are in ns

2 Timing values shown are for links at 20 Mbits/s

Figure 4.7 IMS C004 link timing

5 Switch implementation

The IMS C004 is internally organised as a set of thirty-two 32 to 1 multiplexors. Each multiplexor has associated with it a six bit latch, five bits of which select one input as the source of data for the corresponding output. The sixth bit is used to connect and disconnect the output. These latches can be read and written by messages sent on the configuration link via **ConfigLinkIn** and **ConfigLinkOut**.

The output of each multiplexor is synchronised with an internal high speed clock and regenerated at the output pad. This synchronisation introduces, on average, a 1.75 bit time delay on the signal. As the signal is not electrically degraded in passing through the switch, it is possible to form links through an arbitrary number of link switches.

Each input and output is identified by a number in the range 0 to 31. A configuration message consisting of one, two or three bytes is transmitted on the configuration link. The configuration messages sent to the switch on this link are shown in table 5.1. If an unspecified configuration message is used, the effect of it is undefined.

Configuration Message	Function
[0] [input] [output]	Connects **input** to **output**
[1] [link1] [link2]	Connects **link1** to **link2** by connecting the input of **link1** to the output of **link2** and the input of **link2** to the output of **link1**.
[2] [output]	Enquires which input the **output** is connected to. The IMS C004 responds with the input. The most significant bit of this byte indicates whether the output is connected (bit set high) or disconnected (bit set low).
[3]	This command byte must be sent at the end of every configuration sequence which sets up a connection. The IMS C004 is then ready to accept data on the connected inputs.
[4]	Resets the switch. All outputs are disconnected and held low. This also happens when **Reset** is applied to the IMS C004.
[5] [output]	Output **output** is disconnected and held low.
[6] [link1] [link2]	Disconnects the output of **link1** and the output of **link2**.

Table 5.1 IMS C004 configuration messages

6 Applications

6.1 Link switching

The IMS C004 provides full switching capabilities between 32 INMOS links. It can also be used as a component of a larger link switch. For example, three IMS C004s can be connected together to produce a 48 way switch, as shown in figure 6.1. This technique can be extended to the switch shown in figure 6.2.

A fully connected network of 32 transputers (one in which all four links are used on every transputer) can be completely configured using just four IMS C004s. Figure 6.5 shows the connected transputer network.

In these diagrams each link line shown represents a unidirectional link; i.e. one output to one input. Where a number is also given, that denotes the number of lines.

6.2 Multiple IMS C004 control

Many systems require a number of IMS C004's, each configured via its own configuration link. A simple method of implementing this uses a master IMS C004, as shown in figure 6.3. One of the transputer links is used to configure the master link switch, whilst another transputer link is multiplexed via the master to send configuration messages to any of the other 31 IMS C004 links.

6.3 Bidirectional exchange

Use of the IMS C004 is not restricted to computer configuration applications. The ability to change the switch setting dynamically enables it to be used as a general purpose message router. This may, of course, also find applications in computing with the emergence of the new generation of supercomputers, but a more widespread use may be found as a communication exchange.

In the application shown in figure 6.4, a message into the exchange must be preceded by a destination token *dest*. When this message is passed, the destination token is replaced with a source token so that the receiver knows where the message has come from. The **in.out** device in the diagram and the controller can be implemented easily with a transputer, and the link protocol for establishing communication with these devices can be interfaced with SGS-THOMSON link adaptors. All messages from **rx[i]** are preceded by the destination output *dest*. On receipt of such a message the **in.out** device requests the controller to connect a bidirectional link path to *dest*. The controller determines what is currently connected to each end of the proposed link. When both ends are free it sets up the IMS C004 and informs both ends of the new link. Note that in this network two channels are placed on each IMS C004 link, one for each direction.

6.4 Bus systems

The IMS C004 can be used in conjunction with the IMS C011/C012 link adaptors to provide a flexible means of connecting conventional bus based microprocessor systems.

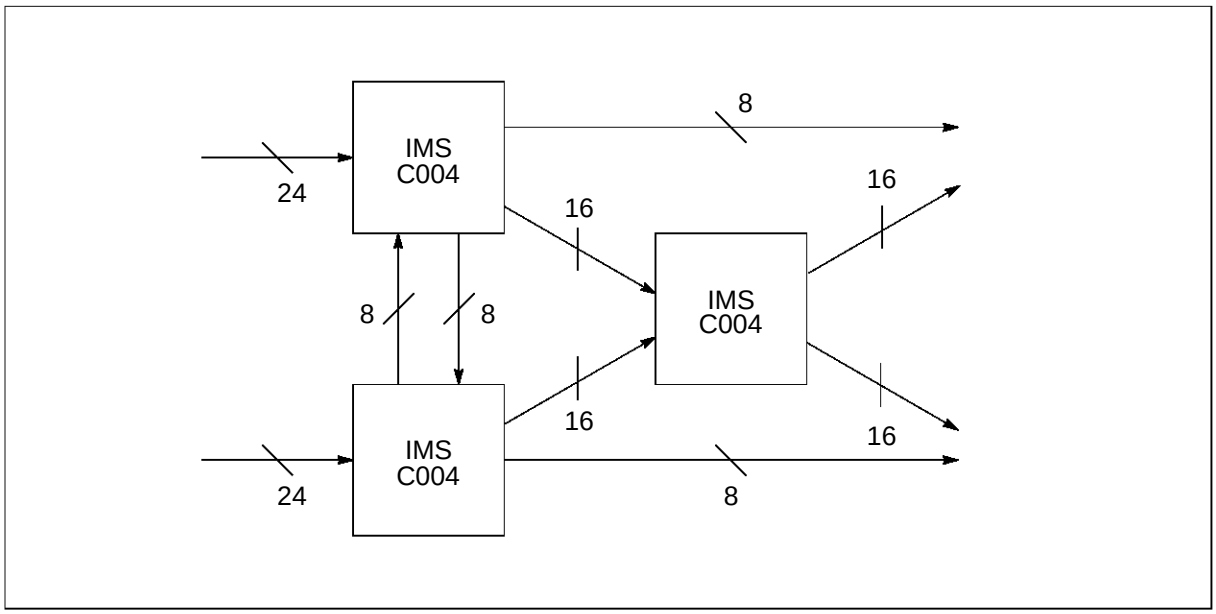


Figure 6.1 48 way link switch

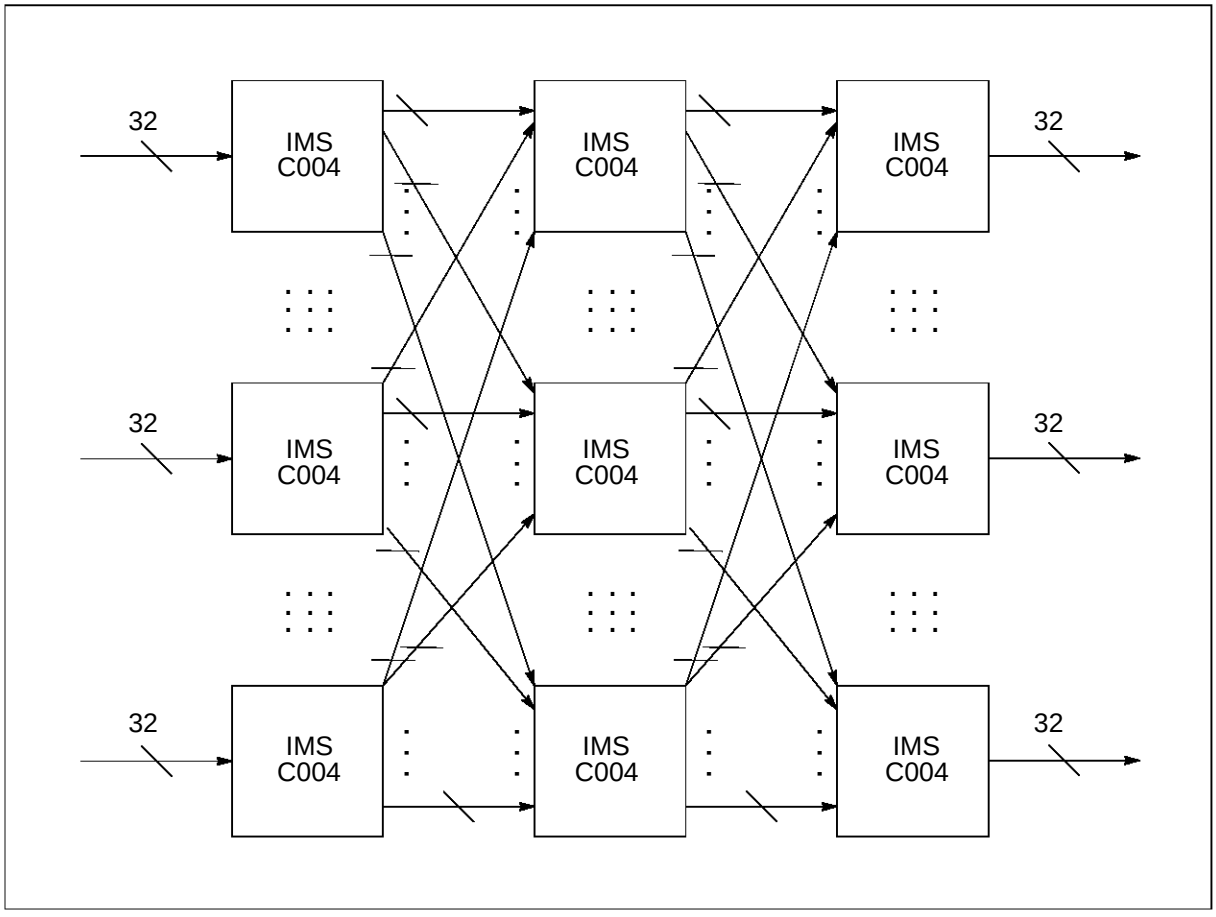


Figure 6.2 Generalised link switch

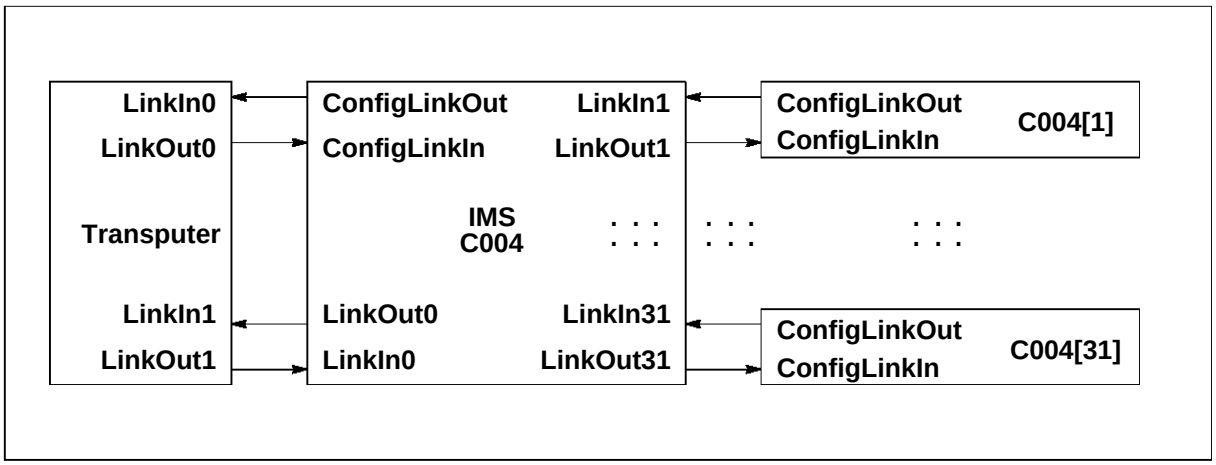


Figure 6.3 Multiple IMS C004 controller

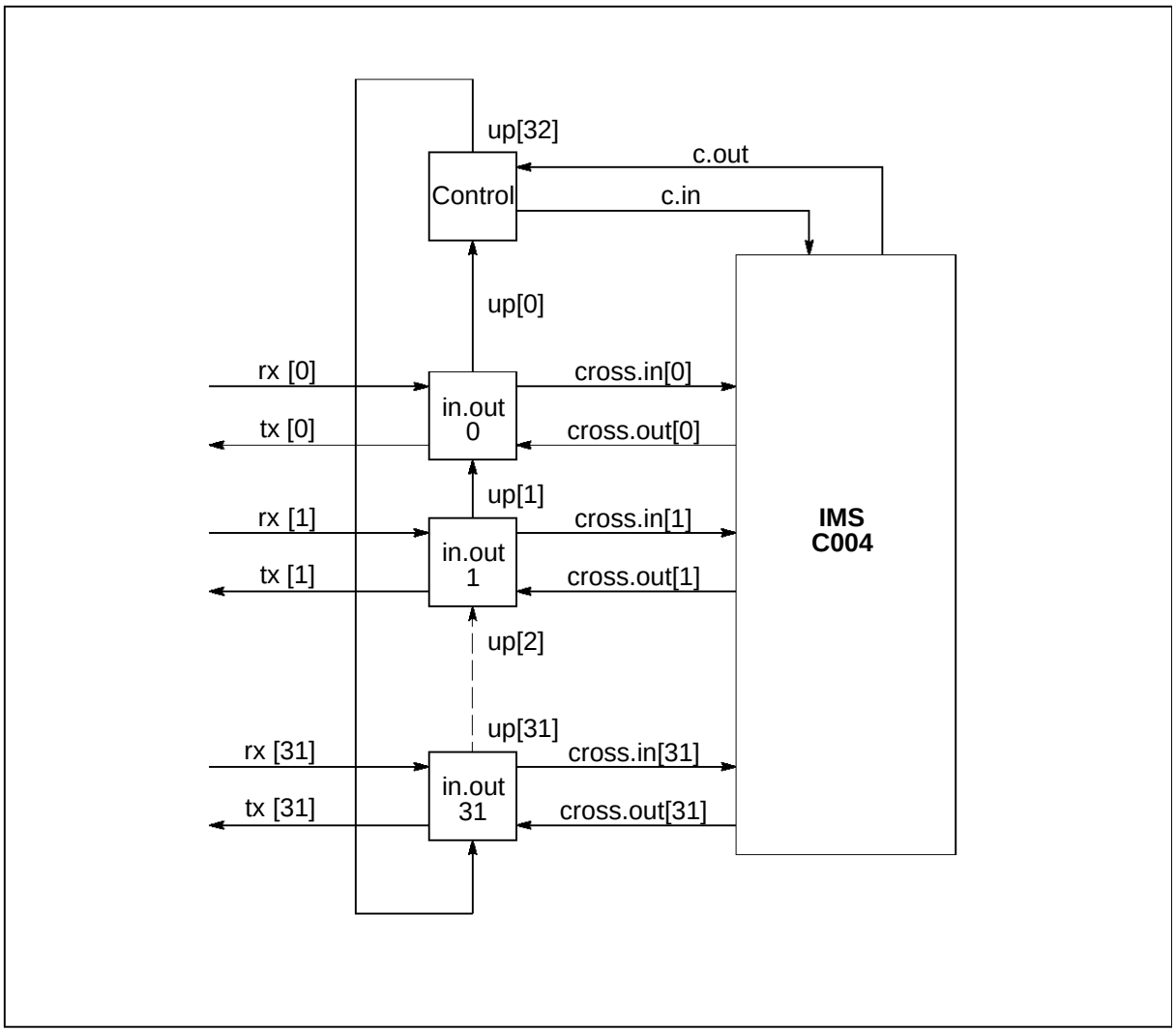


Figure 6.4 32 way bidirectional exchange

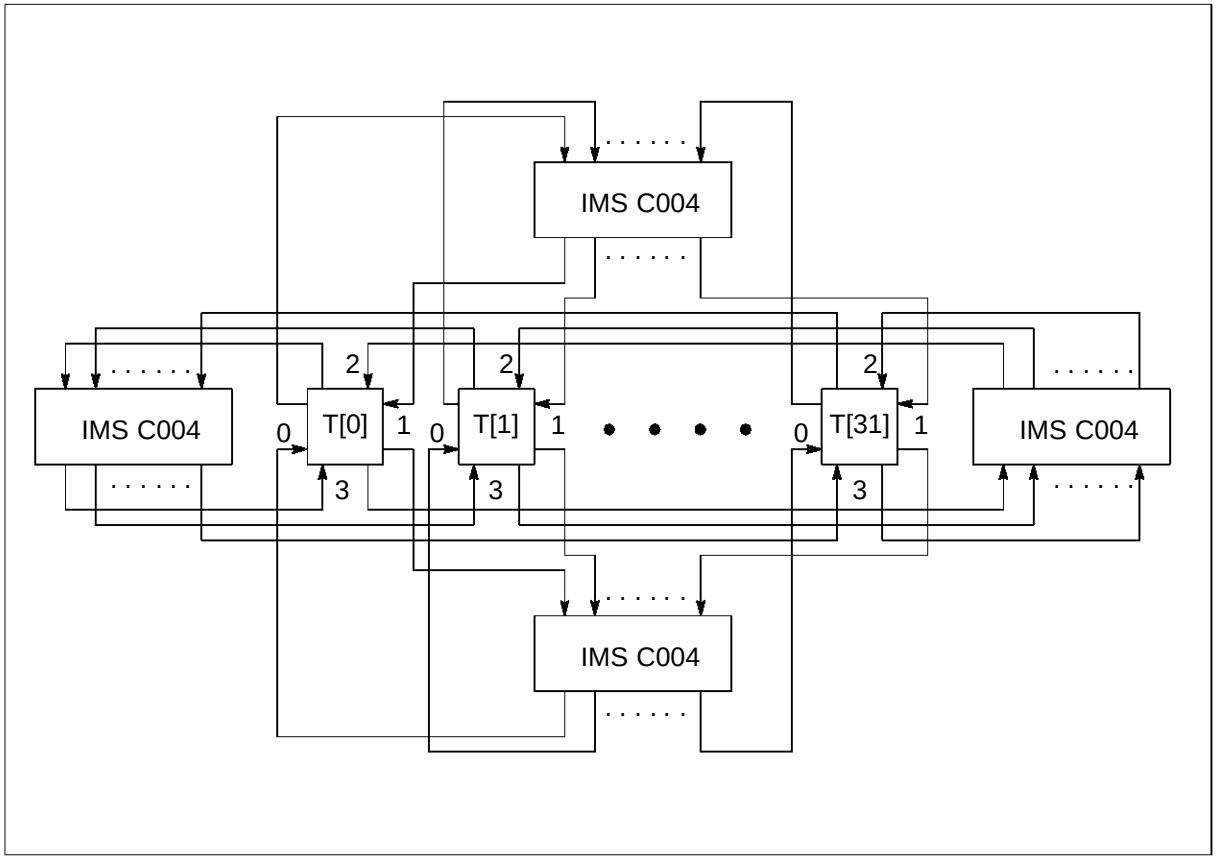


Figure 6.5 Complete connectivity of a transputer network using four IMS C004s

7 Electrical specifications

7.1 DC electrical characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VDD	DC supply voltage	0	7.0	V	1, 2, 3
VI, VO	Voltage on input and output pins	–0.5	VDD+0.5	V	1, 2, 3
II	Input current		25	mA	4
OSCT	Output short circuit time (one pin)		1	s	2
TS	Storage temperature	–65	150	_C	2
TA	Ambient temperature under bias	–55	125	_C	2
PDmax	Maximum allowable dissipation		2	W	

Notes

1 All voltages are with respect to **GND**.

2 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Unused inputs should be tied to an appropriate logic level such as **VDD** or **GND**.

4 The input current applies to any input or output pin and applies when the voltage on the pin is between **GND** and **VDD**.

Table 7.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD	DC supply voltage	4.75	5.25	V	1
VI, VO	Input or output voltage	0	VDD	V	1,2
CL	Load capacitance on any pin		60	pF	
TA	Operating temperature range	0	70	_C	3

Notes

1 All voltages are with respect to **GND**.

2 Excursions beyond the supplies are permitted but not recommended; see DC characteristics.

3 Air flow rate 400 linear ft/min transverse air flow.

Table 7.2 Operating conditions

Symbol	Parameter		Min	Max	Unit	Notes
VIH	High level input voltage		2.0	VDD+0.5	V	1,2
VIL	Low level input voltage		–0.5	0.8	V	1,2
II	Input current	@ GND<VI<VDD		10	mA	1,2
VOH	Output high voltage	@ IOH=2mA	VDD–1		V	1,2
VOL	Output low voltage	@ IOL=4mA		0.4	V	1,2
PD	Power dissipation			1.5	W	2,3
CIN	Input capacitance	@ f=1MHz		7	pF	
COZ	Output capacitance	@ f=1MHz		10	pF	

Notes

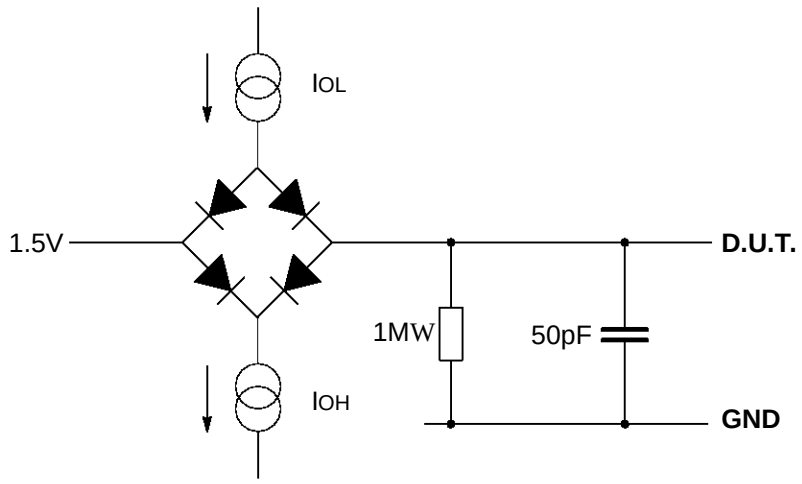
1 All voltages are with respect to **GND**.

2 Parameters for IMS C004–S measured at 4.75V<**VDD**<5.25V and 0°C<**TA**<70°C. Input clock frequency = 5 MHz.

3 Power dissipation varies with output loading and with the number of links active.

Table 7.3 DC characteristics

7.2 Equivalent circuits



Note: This circuit represents the device sinking IOL and sourcing IOH with a 50pF capacitive load.

Figure 7.1 Load circuit for AC measurements

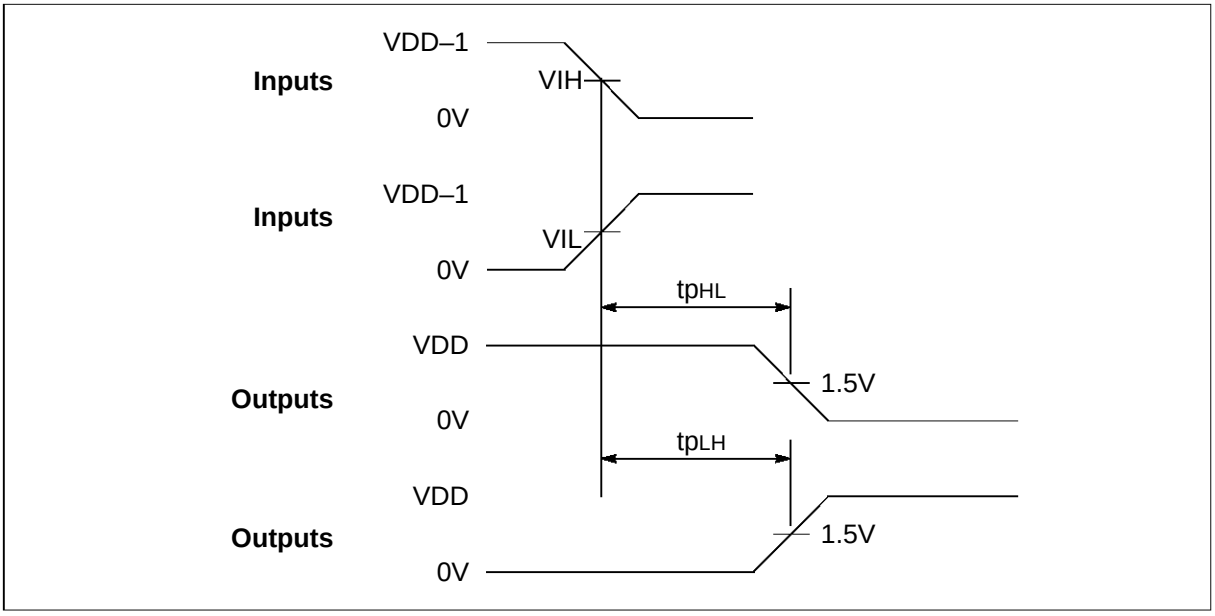


Figure 7.2 AC measurements timing waveforms

7.3 AC timing characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
TDr	Input rising edges	2	20	ns	1, 2
TDf	Input falling edges	2	20	ns	1, 2

Notes

1 Non-link pins; see section on links.

2 All inputs except **ClockIn**; see section on **ClockIn**.

Table 7.4 Input and output edges

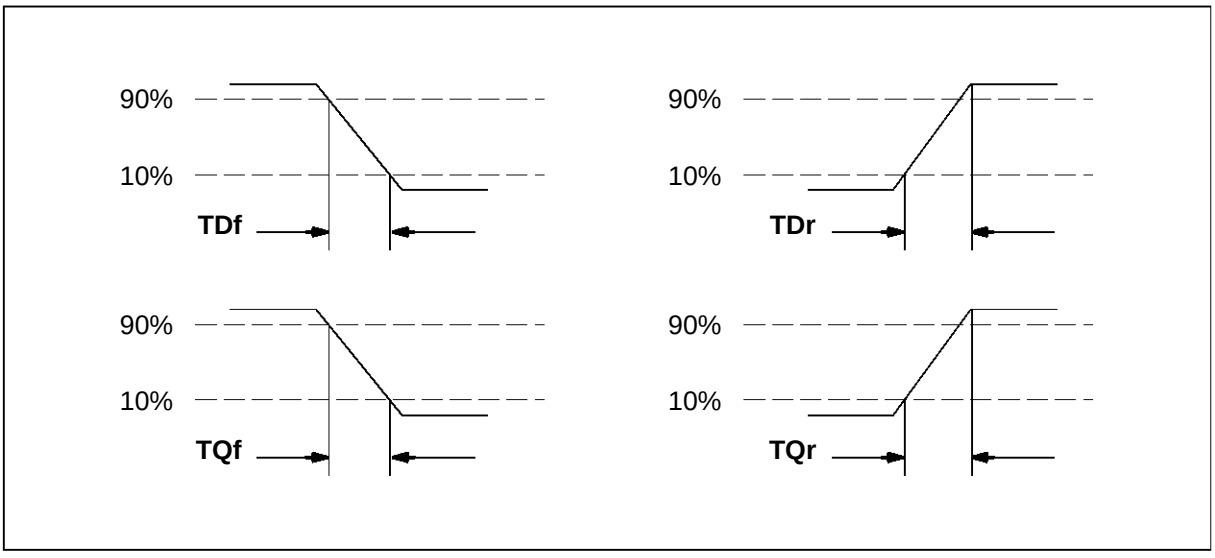


Figure 7.3 IMS C004 input and output edge timing

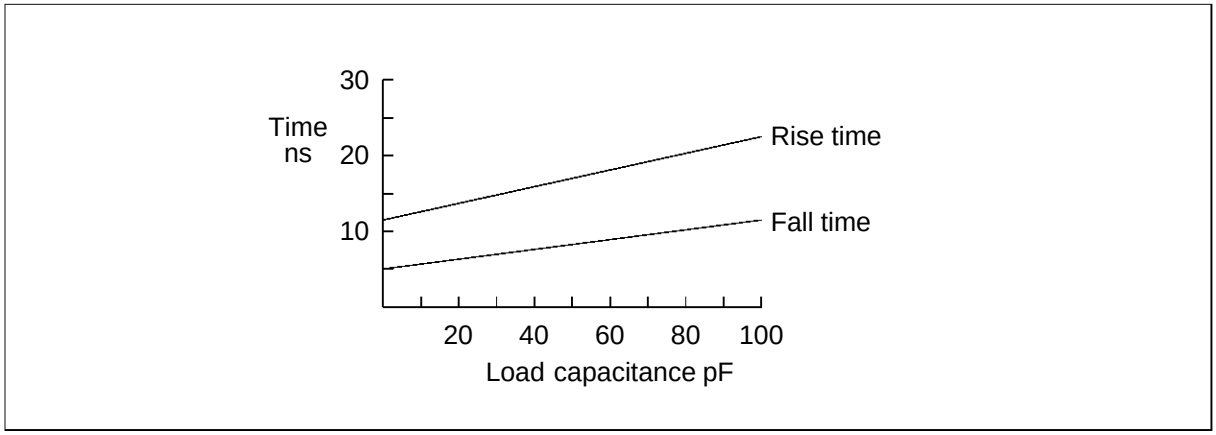


Figure 7.4 Typical link rise/fall times

7.4 Power rating

Internal power dissipation P_{INT} of transputer and peripheral chips depends on VDD, as shown in figure 7.5. P_{INT} is substantially independent of temperature.

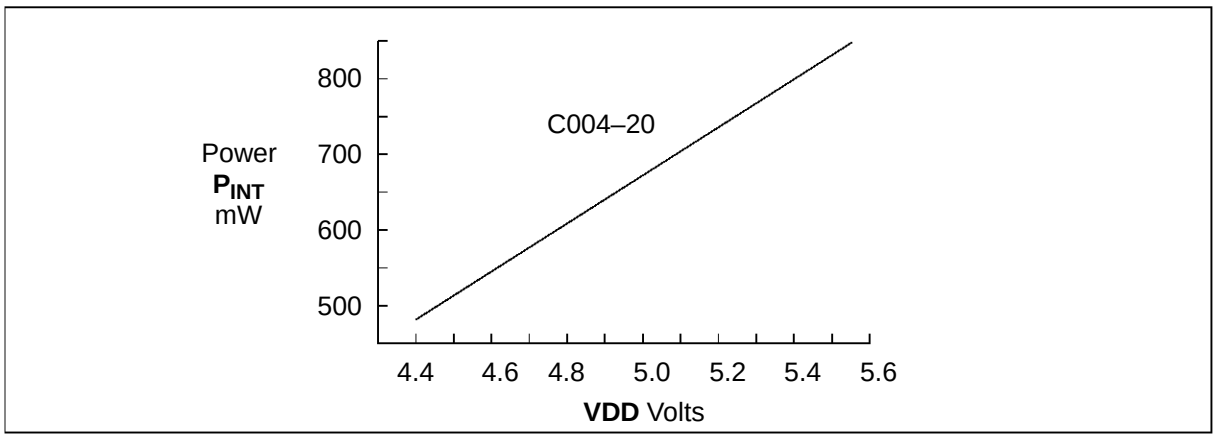


Figure 7.5 IMS C004 internal power dissipation vs VDD

Total power dissipation P_D of the chip is:

$$P_D = P_{INT} + P_{IO}$$

Where P_{IO} is the power dissipation in the input and output pins; this is application dependent.

Internal working temperature T_J of the chip is:

$$T_J = T_A + qJ_A * P_D$$

where T_A is the external ambient temperature in ^oC and q_{JA} is the junction-to-ambient thermal resistance in $^oC/W$.

Further information about device thermal characteristics can be found in section 8.1.

8 Package details

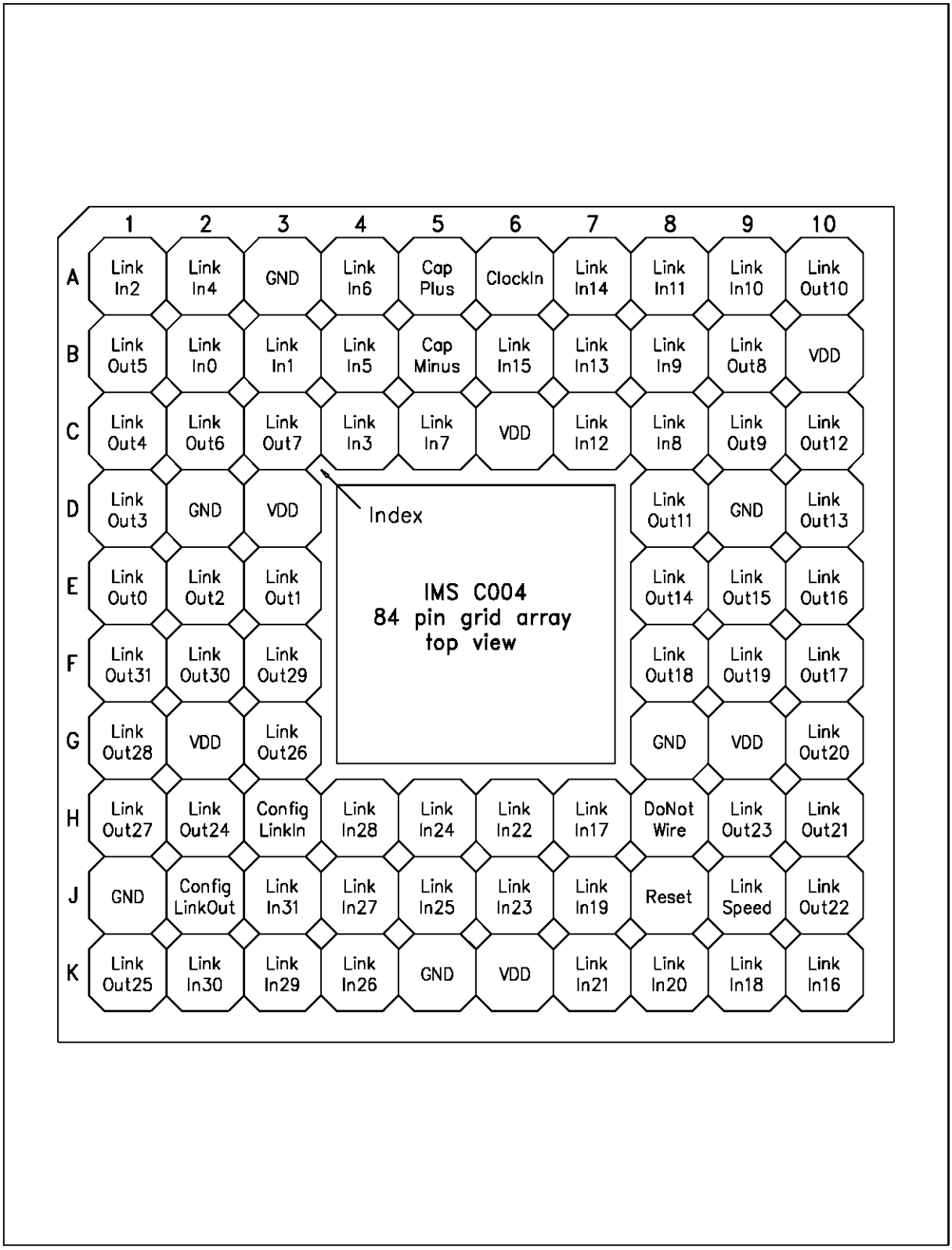


Figure 8.1 IMSC004 84-pin grid array (PGA) package pinout

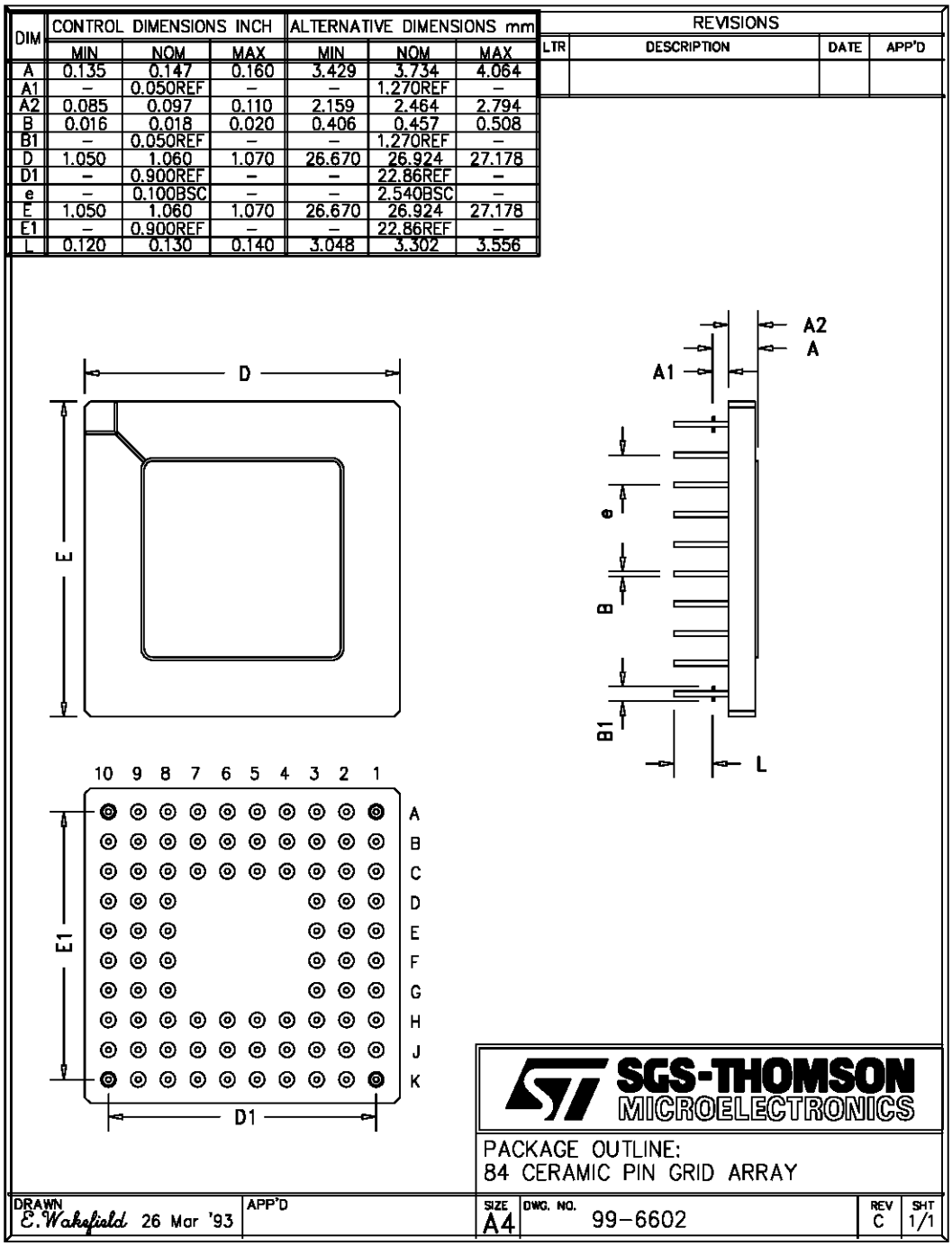


Figure 8.2 IMSC004 84-pin grid array (PGA) package dimensions

8.1 Thermal specification

The IMS C004 is tested to a maximum silicon temperature of 100_C. For operation within the given specifications, the case temperature should not exceed 85_C.

For temperatures above 85_C the operation of the device cannot be guaranteed and reliability may be impaired.

For further information on reliability refer to the SGS–THOMSON Microelectronics Quality and Reliability Program.

9 Ordering

This section indicates the designation of package selections for the IMS C004. Speed of **ClockIn** is 5 MHz for all parts.

For availability contact your local SGS–THOMSON sales office or authorized distributor.

SGS–THOMSON designation	Package
IMS C004-G20S	84 pin ceramic pin grid array

Table 9.1 IMS C004 ordering details