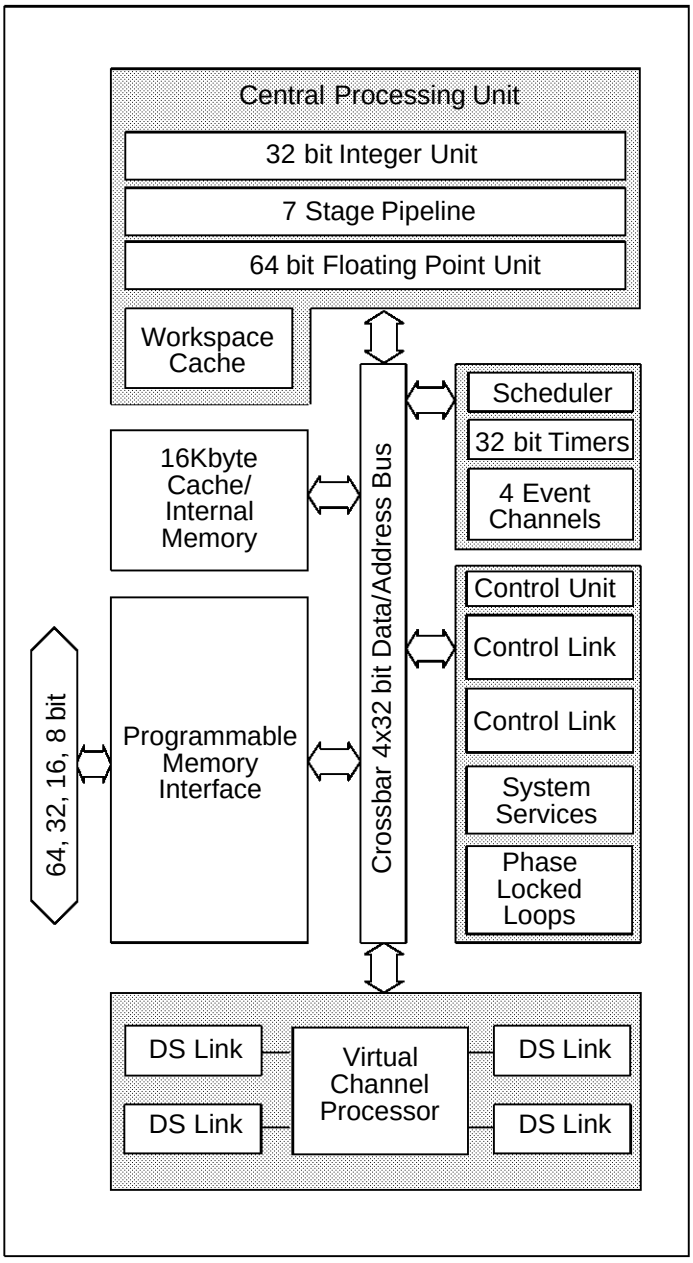
SGS-THOMSON MICROELECTRONICS

IMS T9000

32 BIT MICROPROCESSOR

FEATURES

- Pipelined superscalar micro-architecture
- Workspace cache
- Programmable memory interface
- 4 Gbyte physical address space
- 16 Kbyte instruction and data cache
- 120 MIPS peak
- >80 MIPS sustained
- >7 MFLOPs sustained
- Sub-microsecond interrupt response
- Per process error handling
- Enhanced support for pre-emptive schedulers
- Memory protection and address translation
- 64 K virtual communication links
- Support for message routing
- Unidirectional peak bandwidth of 10 Mbytes/s per link
- Separate control system
- Single 5 MHz clock input
- 20 MHz clock speed
- 208 pin CLCC package
- Single 5 V 5% power supply



Contents

Instruction Set

FP instructions

The following floating point instructions are not fully supported: *fpi32tor32*, *fpchki32*, *fpchki64*, *fpint*, *fprtoi32*, *fpstnli32*, *fprem*, *fprange*, *fpeq*, *fplg*, *fple*, *fpgt*, *icl*, *fdcl*, *ica*, *fdca*, *eqc 0*. Workarounds are present in all SGS-THOMSON T9000 compilers which make this transparent to users.

References: INSdi03119 INSdi03047 INSdi03021 INSdi03171

causeerror and *syscall*

The instructions *causeerror* and *syscall* save an incorrect **Iptr** when executed in a process with a null trap handler.

Reference: INSdi03817

devmove

The *devmove* instruction may malfunction where the source address is not aligned on a word boundary and the source and destination do not have the same alignment. In this situation, device load and store instructions must be used instead.

Reference: INSco00056

sttimer

An attempt to use the *sttimer* instruction to set the CPU Timer may set an incorrect value. If it is necessary to set a specific value, the value should be read back after writing, checked, and rewritten until it is correct.

Reference: INSco00057

crcword, *crcbyte*

CRC instructions *crcword*, *crcbyte* require a software workaround to adjust the operands immediately before the relevant instruction is used.

Reference: INSco00058

fpldall

fpldall requires that any single precision numbers are duplicated in both high and low words. This condition is met by *fpstall*.

Reference: INSco00060

fpdiv

In rare circumstances, the fpdiv instruction has been observed to return an incorrect result. If users experience a problem they are advised to avoid *fpdiv* or if not possible to contact support.

Reference: INSco00071

Communications

HdrAreaBase register after reset 2

After a reset 2 operation, the VCP HdrAreaBase register is reset rather than remaining unchanged, and so must be reprogrammed.

Reference: INSdi03508

HeaderAreaBase read address

In order to read the HeaderAreaBase register, the config address #0801 should be used rather than #0901. Values should still be *written* to address #0901.

Reference: INSdi03468

Event channels in ALTs

Event channels cannot be used as selecting inputs in ALT constructs.

Reference: INSdi03813

sethdr instruction

The *sethdr* instruction will only program virtual channels with headers shorter than 4 bytes.

Reference: INSdi04058

Reset 2

After reset 2 or a DS-Link reset, the VCP may fail to send the first outgoing packet, which may cause deadlock. Correct behavior is assured if the LocalizeError bit in each link is cleared before reset 2.

Reference: INSdi04165

DS-Link reset

A DS-Link connection can fail to be reset correctly with a single ResetLink command. The workaround is to reset the link twice within 3.2 microseconds which requires the use of *stconf*, *resetch*, or *setchmode*.

Reference: INSco00052

DS-Link input

The DS-Link input will ignore the first falling edges after reset. Therefore the link outputs of the other device should be reset low.

Reference: INSco00059

Virtual resource channels

Virtual resource channels require a workaround: the server should guard the granting of the resource channel with an ALT.

Reference: INSco00063

Control Link return header

The Control Link return header may be corrupted if RecoverError is used while Start is in progress.

Reference: INSco00066

Memory system

doallocate instruction

The *doallocate* instruction is not fully supported.

Reference: INSdi04166

Multiple error generation

The EMI can generate four EmiErrors in response to a single error when *doallocate* is applied to an illegal address.

Reference: INSco00053

Reset 2

After a reset 2, a read to an uncacheable location (i.e. a location not in device-only memory) should be made before sending a ‘Run’.

Reference: INSco00051

MemWait

In the first cycle of MemWait being asserted, any configured transition on the Write strobes will nevertheless occur.

Reference: INSsy00063

Databus active during BusReleaseTime

The T9000 may erroneously drive the databus during BusReleaseTime.

Reference: INSsy00100

MemWait incorrect in penultimate cycle

MemWait cannot be used in the penultimate cycle of an access to a bank configured to have a non zero precharge time. The workaround is to extend the memory access time by one cycle, so that MemWait is not asserted in the penultimate cycle.

Reference: INSco00055

Illegal accesses

The IMS T9000 may make speculative accesses to illegal locations. These may cause an error and therefore Bank 3 should be configured to cover all addresses. It is possible that the access made is to a device bank, see below.

Reference: INSco00062

Unprotected device banks

The setting of device banks may not protect from non device accesses. This includes the possibility of speculative accesses being made to a device.

Reference: INSco00064

Miscellaneous

ajw, *gajw* instructions

P process address protection will not cause a trap when either of the instructions *ajw* or *gajw* accesses an illegal address. A trap will however occur on a subsequent illegal access.

Reference: INSdi03022

IEEE values

IEEE denormalized and NaN values are not supported (truncated to zero). Rounding mode is always set to round to nearest.

Reference: INSdi03119

Write locking of configuration registers

Write locking of the configuration registers is not implemented.

Reference: INSdi04167

Reset 3

Reset 3 may fail to place the CPU in a runnable state if a CPU error or other global error has occurred, despite returning a handshake indicating success. Reset 2 should be used in this case.

Reference: INSco00018

Jump 0

Jump 0 breakpoints may be reported as memory semantics errors.

Reference: INSco00061

1 IMS T9000 introduction

The IMS T9000 transputer is a 32-bit CMOS microprocessor designed to be used in applications which require high performance combined with high integration and simplicity of use. Software support for the IMS T9000 transputer includes ANSI C compilers and occam toolsets developed and supported by SGS-THOMSON.

Figure 1.1 shows the major operational units of the IMS T9000 transputer.

The IMS T9000 has a pipelined superscalar architecture, which allows multiple instructions to be executed every processor cycle. Compilers can generate code without considering any details of the pipeline as the hardware organizes the incoming instruction stream into optimum groups of instructions. Other features which contribute to performance are a 16 Kbyte instruction and data cache, a 64-bit floating point unit, and a high bandwidth programmable memory interface. A separate workspace cache stores 32 locations relative to the workspace pointer to provide zero latency access to local variables. The IMS T9000 has four communication links for fast inter-processor communications.

The FPU provides single and double length arithmetic. The IMS T9000 running at a processor speed of 20 MHz is able to perform floating point operations at a rate of 7 Mflops sustained.

The 16 Kbyte cache provides a peak bandwidth of 400 Mbytes/sec. It can also be programmed to function as 16 Kbyte of on-chip memory, or as 8 Kbyte of on-chip memory and 8 Kbyte of cache. This allows small applications to run with no external memory, and guarantees deterministic code behavior for applications where this is critical.

The highly integrated programmable memory interface has a 4 Gbyte physical address space, and provides a peak bandwidth of 100 Mbytes/sec. Four independent banks of external memory are supported, and this allows the implementation of mixed memory systems, with support for DRAM, SRAM, EPROM and VRAM. It has a 64-bit data bus, and each bank of memory can be configured to be 8, 16, 32 or 64 bits wide. The full performance of the IMS T9000 can be exploited using low-cost DRAM, and up to 8 Mbytes of DRAM can be connected with no external components.

Transputers provide hardware support for scheduling processes, and this can be used directly by applications written, for example, in C or occam. It can also be used to simplify the software implementation of real-time kernels and operating systems. The process model of the IMS T9000 transputer provides per process error handling and debugging support, and allows programs to be run in a protected logical address space. To improve the efficiency of real-time kernels access to the state of the processor has been simplified, and full control over interrupts and timeslicing has been provided.

Communication between processes takes place over channels, and is implemented in hardware. The same machine instructions are used for communication between processes on the same processor as for communication between processes on different IMS T9000 processors. On the IMS T9000, communication between processes on different processors takes place over *virtual* channels. Virtual channels are multiplexed onto each physical link by the virtual channel processor. Communication between IMS T9000 transputers that are not directly connected is achieved by using a separate asynchronous packet switch, the STC104.

With virtual channels it is not necessary for the programmer to allocate channels to physical links, and the allocation of processes to processors is simplified. The programming of powerful multiprocessor systems is therefore flexible and elegant.

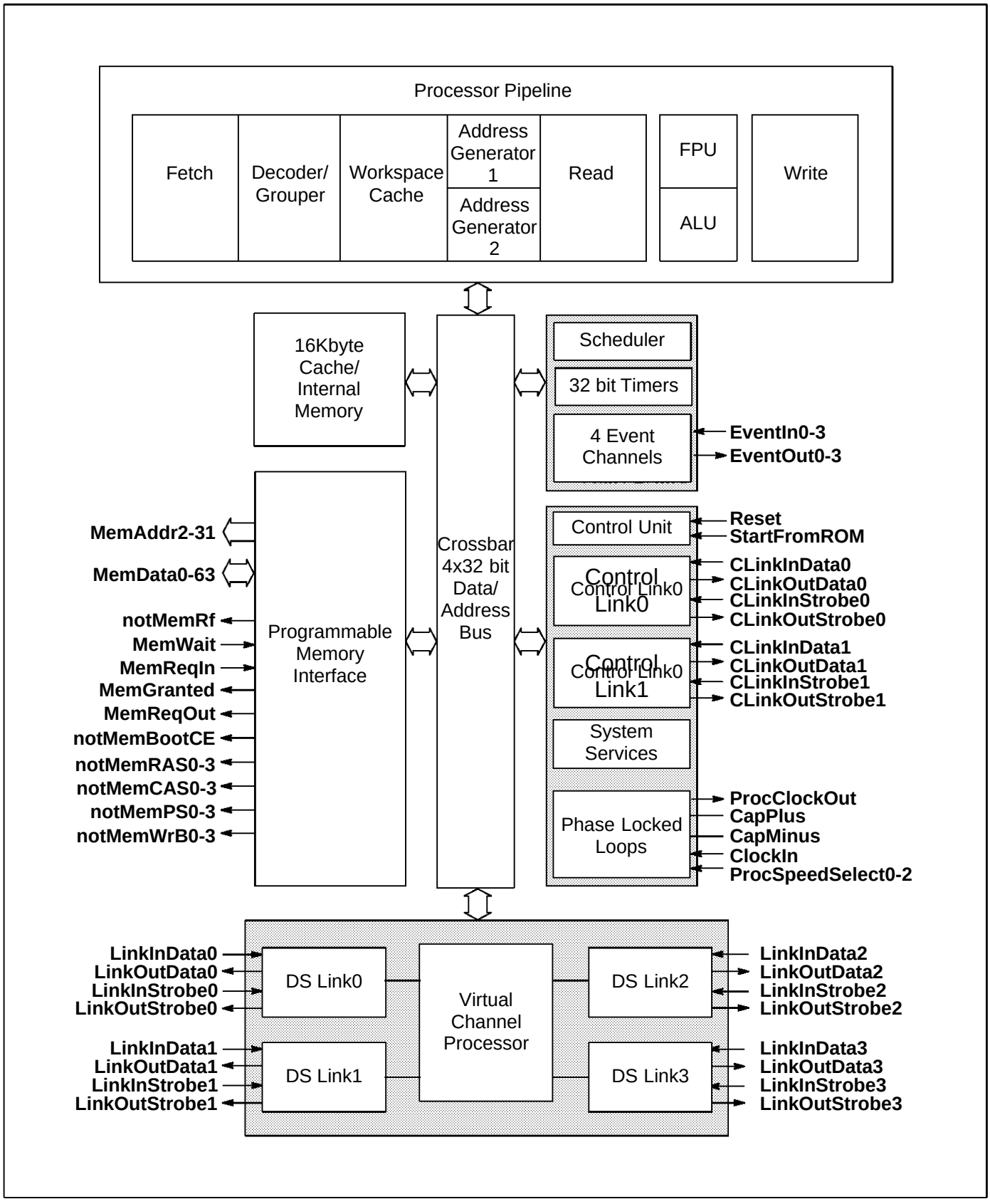


Figure 1.1 IMS T9000 block diagram

The IMS T9000 has four high-bandwidth serial communication links which support virtual channels and dynamic message switching and provide a high data bandwidth with high data integrity. Each physical link consists of four wires, two in each direction, one carrying data and one carrying a strobe. The links are therefore referred to as data-strobe (DS-Links). The four DS-Links support a total bidirectional data bandwidth of 40 Mbytes/sec.

Two separate control links are provided to enable networks of IMS T9000 processors to be controlled and monitored for errors, even during the presence of faults in the normal data communications network. The control links of IMS T9000s and STC104s can be daisy chained, and/or connected into a tree by connection to a STC104. Whatever the physical connectivity the controlling network forms a logical tree, and a control processor is connected at its root. For small systems (such as a single IMS T9000 transputer) there is no need to use the control links as all necessary functionality can be controlled from software.

The hardware scheduling mechanism enables the creation and execution of any number of high and low priority processes. It handles timeslicing and message passing, often eliminating the need for a software kernel. Context switch time is sub-microsecond. Two 32-bit clocks tick at 1μs and 64μs intervals. The scheduler provides each process with a timer, simplifying real-time programming.

Four Event I/O pins provide asynchronous handshake interfaces between external events and internal processes and can be used as interrupts or as control for external peripherals. Response time is sub-microsecond.

Two on-chip phase locked loops generate all the internal high frequency clocks from a single clock input, simplifying system design and avoiding problems of distributing high speed clocks externally. The nominal input clock frequency used by all transputer family components is 5 MHz, regardless of device type, transputer word length, or processor cycle time.

2 Pin designations

The following tables outline the function of each of the pins. Pinout details are given in Chapter 10, *Package specifications*.

Signal names are prefixed by **not** if they are active low, otherwise they are active high.

Supplies

Pin	In/Out	Function
VDD		Power supply
GND		Ground

Table 2.1 IMS T9000 supplies

Phase locked loops

Pin	In/Out	Function
CapPlus, CapMinus		External capacitor for internal clock power supply
ClockIn	in	Input clock
ProcSpeedSelect0-2	in	Processor speed selectors
ProcClockOut	out	Processor clock

Table 2.2 IMS T9000 phase locked loops

Programmable memory interface

Pin	In/Out	Function
MemAddr2-31	out	Address bus
MemData0-63	in/out	Data bus
notMemRAS0-3	out	RAS strobes – one per bank
notMemCAS0-3	out	CAS strobes – one per bank
notMemPS0-3	out	Programmable strobes – one per bank
notMemWrB0-3 {	out	Byte-addressing write strobes
MemWait	in	Memory cycle extender
MemReqIn	in	Direct memory access request
MemGranted	out	Direct memory access granted
MemReqOut	out	Processor requires memory bus
notMemBootCE	out	Bootstrap ROM chip enable
notMemRf	out	Dynamic memory refresh indicator

{ these pins have different functions depending on the external port sizes

Table 2.3 IMS T9000 programmable memory interface

Control system

Pin	In/Out	Function
StartFromROM	in	Boot from external ROM or from link
Reset	in	System reset
CLinkInData0-1	in	Control link input data channels
CLinkInStrobe0-1	in	Control link input strobes
CLinkOutData0-1	out	Control link output data channels
CLinkOutStrobe0-1	out	Control link output strobes

Table 2.4 IMS T9000 control system

Communication links

Pin	In/Out	Function
LinkInData0-3	in	Link input data channels
LinkInStrobe0-3	in	Link input strobes
LinkOutData0-3	out	Link output data channels
LinkOutStrobe0-3	out	Link output strobes

Table 2.5 IMS T9000 communication links

Events

Pin	In/Out	Function
EventIn0-3	in	Event inputs
EventOut0-3	out	Event outputs

Table 2.6 IMS T9000 event

Miscellaneous

Pin	In/Out	Function
HoldToGND		Must be connected to **GND**
HoldToVDD		Must be connected to **VDD**
DoNotWire		Must not be wired

Table 2.7 IMS T9000 miscellaneous pins

3 Programmable memory interface

The IMS T9000 programmable memory interface (PMI) can access a 4 Gbyte physical address space, and provides a peak bandwidth of 80 Mbytes/sec at 20MHz. It is designed to support memory subsystems with minimal external support logic. The interface has internal logic to provide decode and timing control functions and can be programmed through the configuration registers.

The external address space is partitioned into four banks (not to be confused with the four cache banks). This allows the implementation of mixed memory systems, with support for DRAM, SRAM, EPROM, VRAM and I/O. The timing of each of the four memory banks can be programmed separately, with a different device type being placed in each bank with no external hardware support. The PMI has a 64 bit data bus, and each bank of memory can be configured to be 8, 16, 32 or 64 bits wide. The PMI directly supports: 8, 16, 32 and 64 bit SRAM; 32 and 64 bit DRAM. All banks programmed to be 64 bit wide memory are defined as cacheable and always transfer a full 64 bit operand to and from external memory to the internal cache, providing fast cache refill. The full performance of the IMS T9000 transputer can be exploited using relatively low-cost DRAM, and up to 8 Mbytes of DRAM can be connected with no external components.

The IMS T9000 PMI has the following features:

- multiplex addressing which replaces the need for an external address multiplexor in DRAM system design
- separate RAS and CAS strobes for each bank
- an extra programmable strobe for each bank
- four write strobes which can be used to write part-words or bytes
- support for DMA accesses.

In this chapter a *cycle* is one processor clock cycle and a *phase* is one quarter of the duration of one processor clock cycle.

3.1 External bus cycles

Transputer memory is byte addressed, with words aligned on eight-byte boundaries for 64 bit devices, four-byte boundaries for 32 bit devices and on two-byte boundaries for 16 bit devices.

During read cycles byte level addressing is performed internally by the IMS T9000. The PMI can read bytes, half-words, words or dual-words. It always reads the size of the bank.

During write cycles the IMS T9000 uses the **notMemWrB0-3** strobes to perform addressing of bytes. If a particular byte is not to be written then the corresponding data outputs are tristated. This allows writes to specified bytes within a word for 16 and 32 bit wide ports, but not for 64 bit wide ports which must always be cached.

The internally generated address is indicated on pins **MemAddr2-31**. However the two low order address bits, **A0-1**, are generated on pins **notMemWrB2-3** respectively as required for 8-bit and 16-bit external data buses.

The least significant bit of the data bus is always **MemData0**. The most significant bit can be adjusted dynamically to suit the required external bus size.

3.1.1 Generic memory cycle

A generic memory interface cycle consists of a number of defined periods, or times, as shown in Figure 3.1. This generic memory cycle uses DRAM terminology to clarify the use of the interface in the most complex situations, but can be programmed to provide waveforms for a wide range of other device types. The timing of each of the four memory banks can be programmed separately, with a different device type being placed in each bank with no external hardware support.

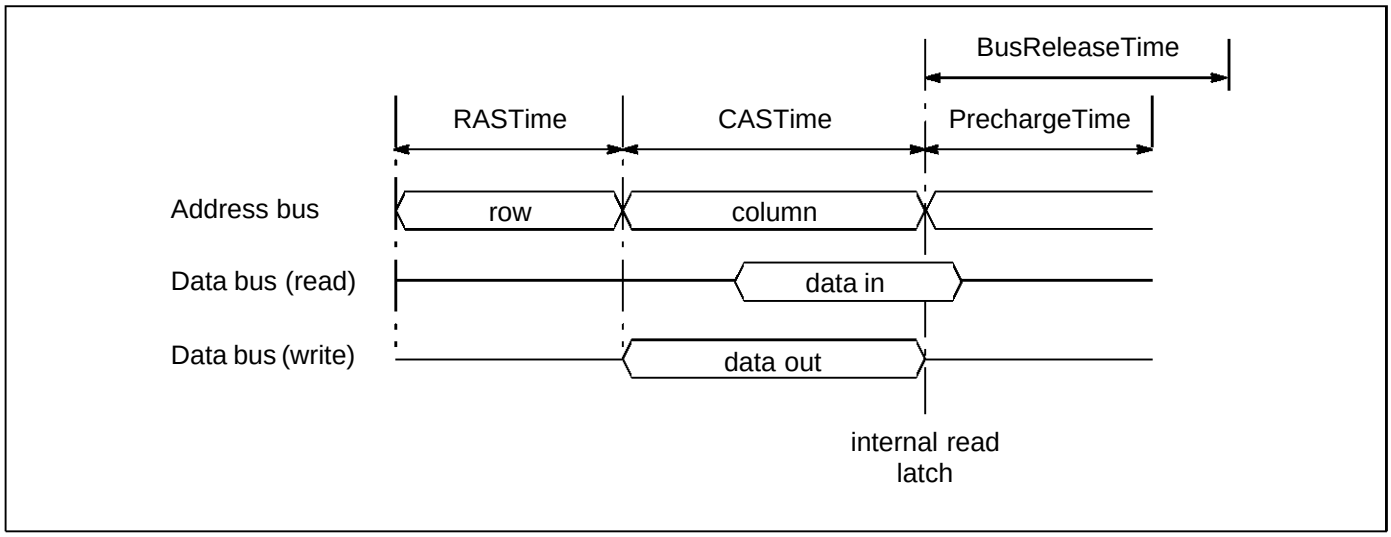


Figure 3.1 Generic memory cycle

The **RASTime** and **CASTime** are consecutive. The **CASTime** can be followed by concurrent **Precharge** and **BusRelease** times. Thus, for DRAM, the times are used for RAS, CAS, and precharge respectively. For non-multiplexed addressed memory the **RASTime** can be programmed to be zero.

If the **RASTime** is programmed to be non-zero, and page-mode memory is programmed in a bank, the **RASTime** will only occur if consecutive accesses are not in the same page. The **RASTime** will not commence until the **PrechargeTime** for a previous access has completed. During this time the address is multiplexed by the amount specified in the format control register for the bank so as to output the row address on the address bus. During the **RASTime** a transition can be programmed on the RAS strobe, but not on any other strobe.

During the **CASTime**, all strobes are active. The address is output on the address bus without being shifted. Write data is valid during **CASTime**. The point at which read data is latched into the interface is referenced to the end of the **CASTime** cycle.

Parametrics are listed in section 3.1.2.

3.1.2 AC timing characteristics

The IMS T9000 PMI has three types of pins; address, data and strobe pins. The falling and rising edges of the strobe pins are programmable through the configuration registers. The following specification is given either as an absolute timing value or as a skew (Dt_{SPEC}) from the nominal programmed number of phases (t_n), where t_n = (nominal programmed number of phases) / (4 * internal clockSpeed). The overall spec value must also be adjusted to take into account the effect of clock variation (caused by the Phase Lock Loop). The amount of clock variation is expressed as

a percentage by the **tPCSTAB** parameter (see Table 6.4). The relationship between the parameter (tSPEC) as specified on the timing diagrams, the skew and the programmed value is as follows:

$$\mathbf{t_{SPEC}} + \mathbf{t_n} \pm \left(\frac{\mathbf{t_n} \times \mathbf{t_{PCSTAB}}}{\mathbf{100}}\right) \pm \mathbf{Dt_{SPEC}} \quad (1)$$

The 'clock variation' component of **tSPEC** is assumed to be the very worst case that can happen, i.e. consecutive clock phases at their shortest or fastest for many clock cycles. This component should be added into the calculation of **tSPEC** to give the worst case value.

The following table gives the data setup and hold times for read, write and wait cycles. It also specifies the maximum skew from the nominal programmed values between the address and strobe pins.

Note, a minimum timing value with a negative value indicates that the transition of the second signal can occur before the first signal. For example the minimum timing specification for address setup to strobe valid is –9ns, i.e. the strobe can be valid 9ns before address setup.

Read cycle

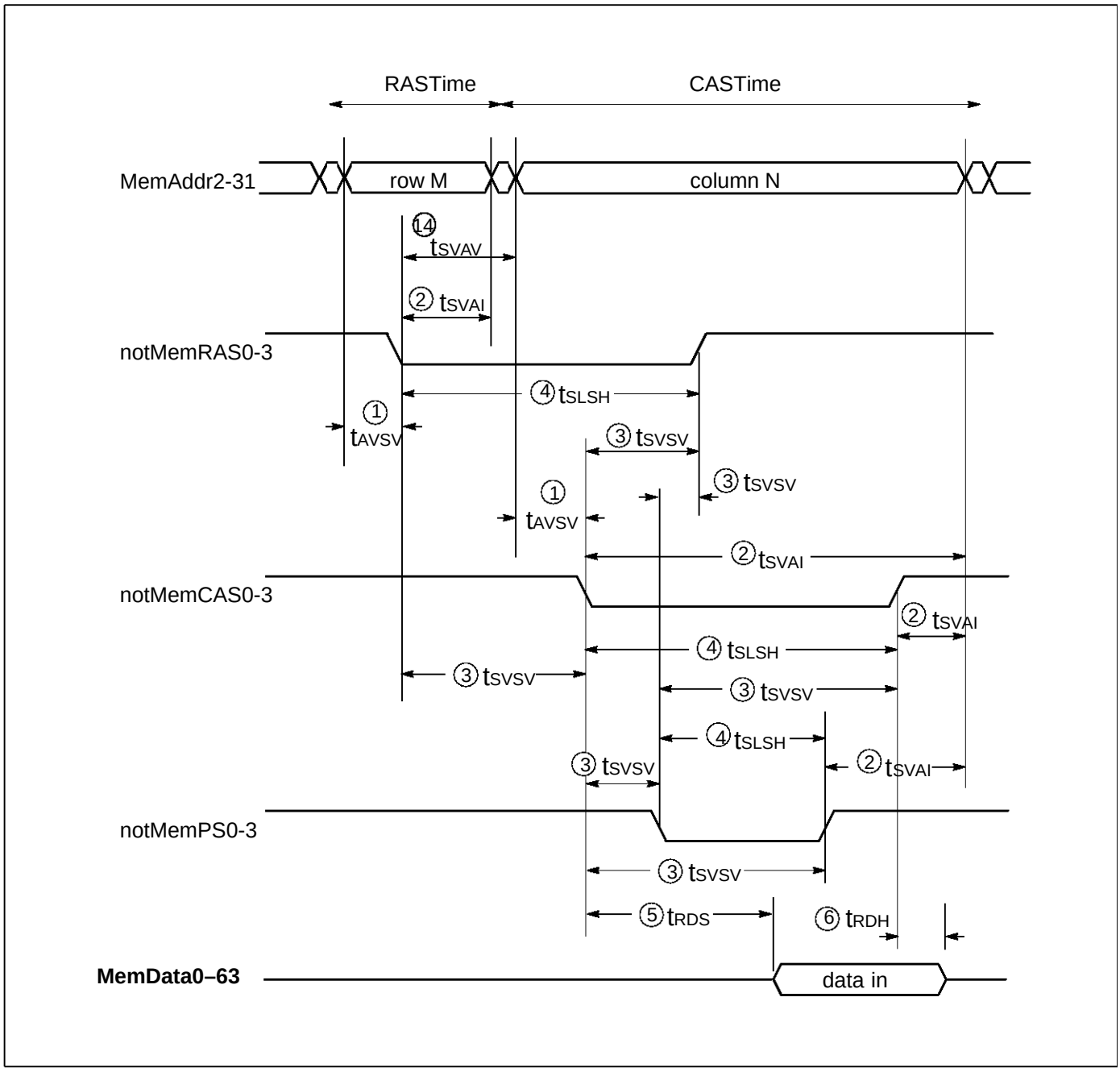


Figure 3.2 Read cycle timing

Write cycle

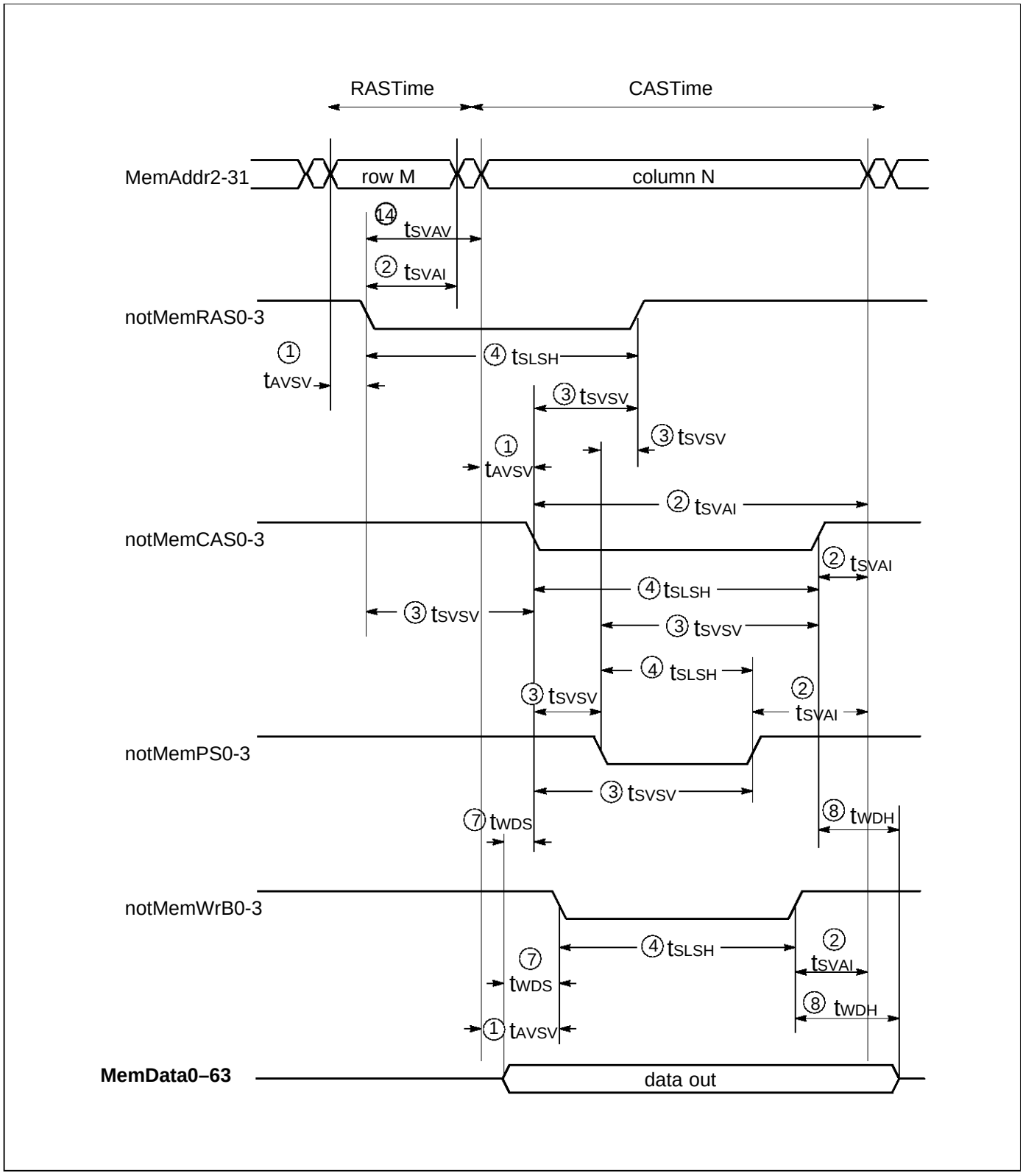


Figure 3.3 Write cycle timing

Consecutive cycles

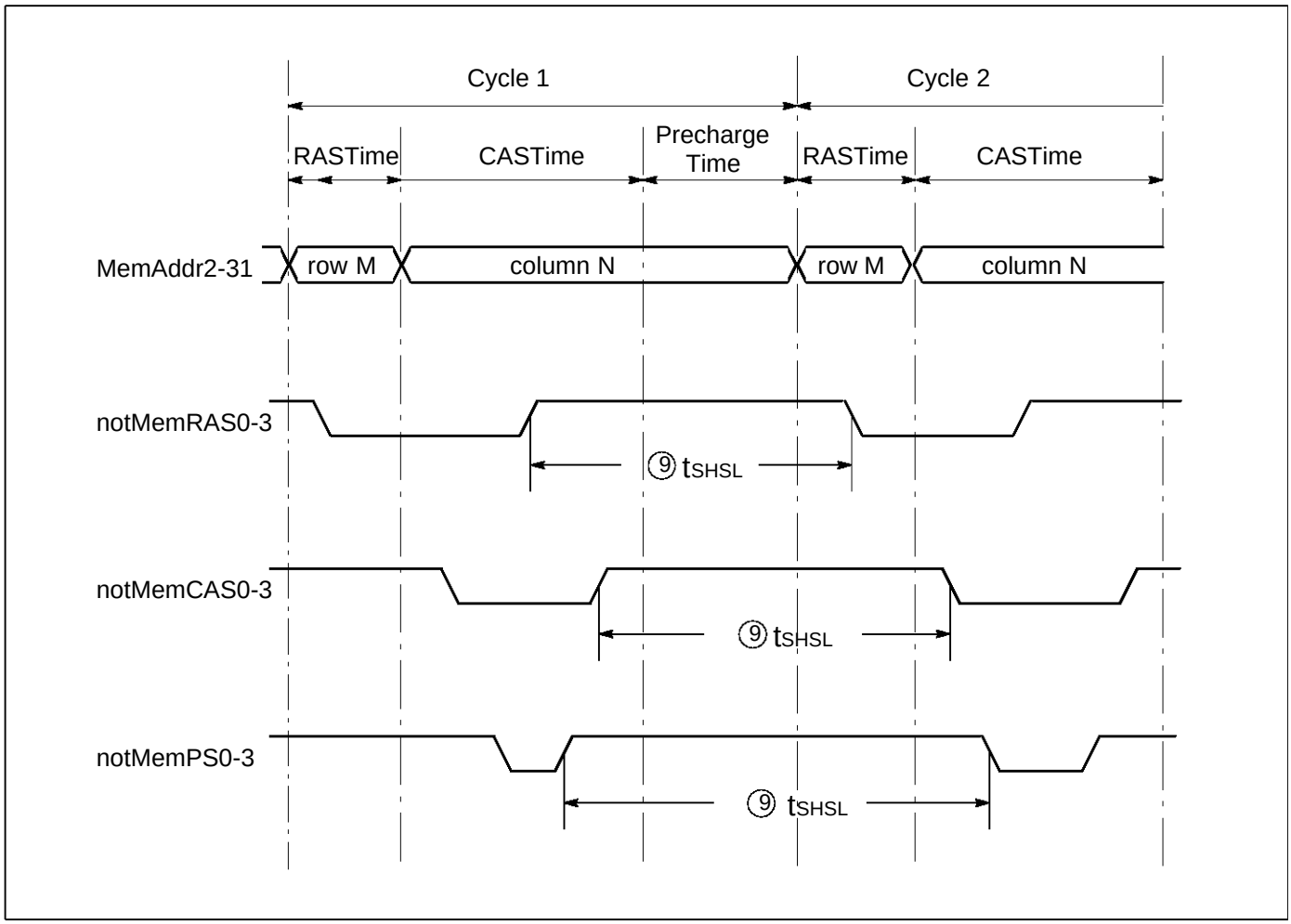


Figure 3.4 Cycle to cycle timing

Symbol	No.	Parameter	Parameter type (see note 1)	Min	Nominal	Max	Units	Notes
Dt_{AVSV}	1	Address setup to strobe valid	skew	–9	–	0	ns	2,3
Dt_{SVAI}	2	Address hold after strobe valid	skew	–3	–	+6	ns	2,3
Dt_{SVSV}	3	Strobe valid to strobe valid	skew	–7	–	+5	ns	2,5
Dt_{SLSH}	4	Strobe low to strobe high	skew	–4	–	+7	ns	2,6
Dt_{SHSL}	9	Strobe high to strobe low	skew	–7	–	+4	ns	2,6
Dt_{SVAV}	14	Strobe valid to next address valid	skew	0	–	+9	ns	2,4
t_{RDS}	5	Read data valid after **notMemCAS** low	nominal	–	(**CASTime**∗4) –$\mathbf{E1Time_{CAS}}$	–	phases	7,8,14
Dt_{RDS}			skew	–	–	–19	ns	
t_{RDH}	6	Read data hold after **notMemCAS** high	nominal	–	(**CASTime**∗4) –$\mathbf{E2Time_{CAS}}$	–	phases	9,10,14
Dt_{RDH}			skew	–5	–	–	ns	
t_{WDS}	7	Write data setup before related strobe low	nominal	–	(**E1Time**–1)	–	phases	11
Dt_{WDS}			skew	–22	–	–	ns	2,12
t_{WDH}	8	Write data hold after related strobe high	nominal	–	(**CASTime**∗4) –**E2Time**	–		13
Dt_{WDH}			skew	–4	–	–	ns	2,12

Table 3.1 PMI AC specifications

Notes

1 *Parameter type*: refer to equation 1 in section 3.1.2 for an explanation of how t_n (nominal programmed value) and Dt_{SPEC} (the skew) are related.

2 The timings are based on the following loading conditions: address pin loaded with 25 pF and strobe pins loaded with 25 pF. All parameters that reference strobe, apply to *all* memory strobes – *eg* **notMemWrB0-3**, **notMemRAS0-3**, **notMemCAS0-3**, **notMemPS0-3**.

3 The value of this parameter is given by the programmed position of the falling edge (**RASEdgeTime** or **E1Time**) of the **RAS**, **CAS** or **PS** strobe.

4 The value of t_{SVAV} is given by the programmed length of the sub-cycle (**RASTime** or **CASTime**) minus the programmed position of the falling strobe edge (**RASEdgeTime** or **E1Time**).

5 The value of t_{SVSV} is given by the absolute difference between any pair of falling edges (**RASEdgeTime** or **E1Time**) or any pair of rising edges (**E2Time**) or any falling to rising pair of strobes.

6 The nominal strobe pulse width (t_{SLSH} or t_{SHSL}) is given by the difference between the programmed falling (**RASEdgeTime** or **E1Time**) and the programmed rising edge (**E2Time**) of a **RAS**, **CAS** or **PS** strobe. This is applicable to a positive or negative pulse.

7 Where $\mathbf{E1Time_{cas}}$ is the programmed falling edge position (**E1Time**) for **notMemCAS** expressed in clock phases.

8 The nominal value of t_{RDS} could be extended by any wait cycles that are inserted after **notMemCAS** goes low. In this case, add 4 phases for every wait cycle.

9 Where $\mathbf{E2Time_{CAS}}$ is the programmed rising edge position (**E2Time**) for **notMemCAS** expressed in clock phases.

10 The nominal value of t_{RDH} could be extended by any wait cycles that are inserted after **notMemCAS** goes high again. In this case, add 4 phases for every wait cycle.

11 The nominal value of t_{WDS} is given by the programmed **E1Time** for **notMemCAS0-3** or **notMemWrB0-3**.

12 Timings are for all four byte write strobes **notMemWrB0-3**.

13 The nominal value of t_{WDH} is given by the programmed **CASTime** ***minus*** the programmed position of the rising edge of **notMemCAS0-3** or **notMemWrB0-3**. Output data may be held indefinitely if there are no subsequent external cycles.

14 These figures are irrespective of the programmed strobe edges as the T9000 subsystems latch data internally and so are not directly related to the programmed strobe timings.

3.2 External DMA

The **MemReqIn** pin high causes the IMS T9000 to tri-state its memory buses so that an external DMA can access memory. **MemReqIn** is sampled during each cycle of **ProcClockOut**, whilst the PMI is idle, or on the last cycle of any external access. If the current cycle is a four-word cache line refill then the four words of the line are read in before the PMI responds. If the cycle is a refresh cycle it is allowed to terminate before the PMI responds. If the current cycle is a word transfer to a smaller port then the interface completes the transfer of the sub-words before responding. **MemGranted** is asserted during the first clock cycle after the current cycle terminates. The address bus, data bus and the strobes are tristated during this clock cycle (see also Figure 3.5).

Deassertion of **MemReqIn** is sampled during each **ProcClockOut** and **MemGranted** is deasserted during the next clock period.

Strobes are tristated during the DMA transfer. If DMA is active for longer than one programmed refresh interval then external logic is responsible for providing refresh.

DMA allows a bootstrap program to be loaded into external memory for execution after reset. If **MemReqIn** is held high during reset, **MemGranted** will be asserted before bootstrapping from external memory begins. The bootstrap sequence will continue when **MemReqIn** is deasserted. This will not prevent bootstrapping from the control links taking place.

The IMS T9000 processor can continue to execute out of the cache until a request to external memory is required. If a DMA operation is in progress then execution will stall until the DMA is complete. The **MemReqOut** indicates to external logic that IMS T9000 external bus cycles are pending and execution has stalled. External logic can use this information to continue or interrupt the DMA transfer in progress.

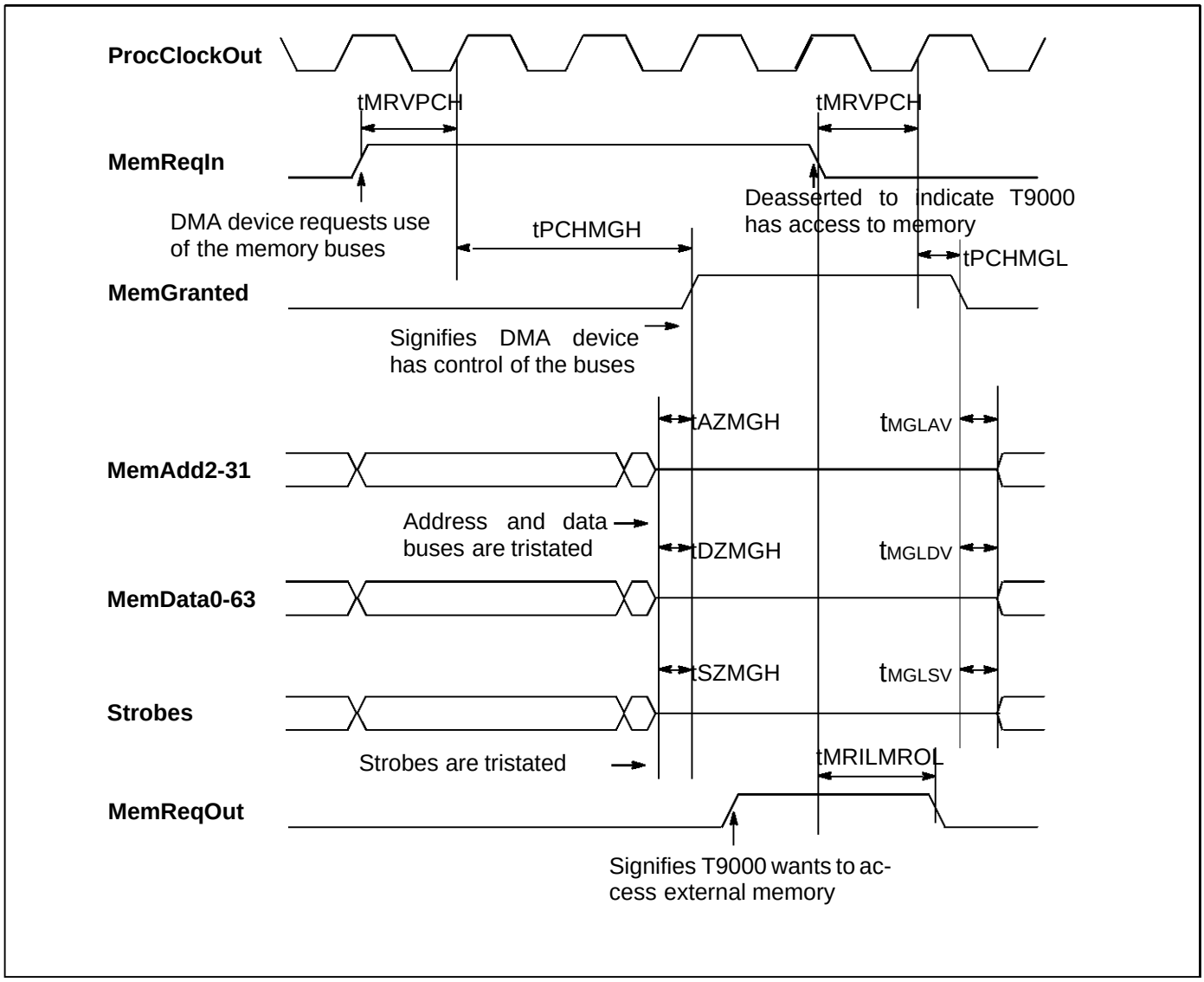


Figure 3.5 DMA

Notes

1 In Figure 3.5 **Strobes** consist of the following signals: **notMemRAS0–3, notMemCAS0–3, notMemPS0–3, notMemRf and notMemBootCE**.

Symbol	Parameter	Parameter type (see note 1)	Min	Nominal	Max	Units	Notes
tMRVPCH	**MemReqIn** setup before **ProcClockOut** rising	absolute	+20	–	–	ns	2
tPCHMGH	**MemReqIn** response time	nominal	–	2	–	cycles	3
DtPCHMGH	**MemReqIn** response time	skew	+9	–	+20	ns	
tPCHMGL	**MemReqIn** end response time	nominal	–	1	–	cycles	
DtPCHMGL	**MemReqIn** end response time	skew	+9	–	+20	ns	
tAZMGH	Address Bus tristate before **MemGranted** high	absolute	0	–	–	ns	
tDZMGH	Data Bus tristate before **MemGranted** high	absolute	0	–	–	ns	
tSZMGH	Strobes Bus tristate before **MemGranted** high	absolute	0	–	–	ns	
tMGLAV	Address Bus active after end of **MemGranted** low	absolute	–	–	5	ns	
tMGLDV	Data Bus active after end of **MemGranted** low	absolute	–	–	5	ns	
tMGLSV	Strobes Bus active after end of **MemGranted** low	absolute	–	–	5	ns	
tMRILMROL	**MemReqOut**	nominal	–	2	–	cycles	
DtMRILMROL	**MemReqOut**	skew	4	–	4	ns	

Table 3.2 Memory request

Notes

1 *Parameter type*: refer to equation 1 in section 3.1.2 for an explanation of how tn (nominal programmed value) and DtSPEC (the skew) are related.

2 Setup time need only be met to guarantee sampling on the following rising edge of **ProcClockOut**.

3 If an external memory cycle is active, the maximum time could be the time taken to complete a (writeback cycle) + (refill cycle) + (refresh cycle), and for any bus release times to complete, where the refill and writeback may read or write up to 32 four bit words, taking the number of cycles determined by the width of the relevant memory bank.

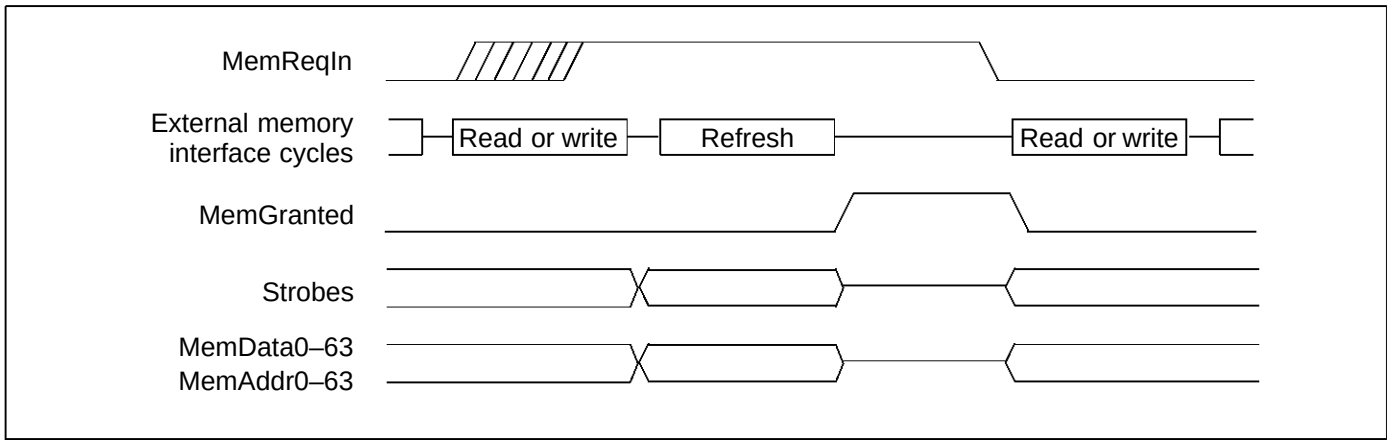


Figure 3.6 IMS T9000 operation of **MemReqIn**, **MemGranted** with external, refresh memory cycles

3.3 Memory refresh

The AC parameters of the strobe edges are equivalent to those defined for the strobes during a read/write cycle as shown in Table 3.1. Another access will not occur until the precharge time for that bank has expired.

notMemRF falls at the beginning of the refresh cycle and rises when the refresh is complete. Its AC parametrics are equivalent to those of the strobes.

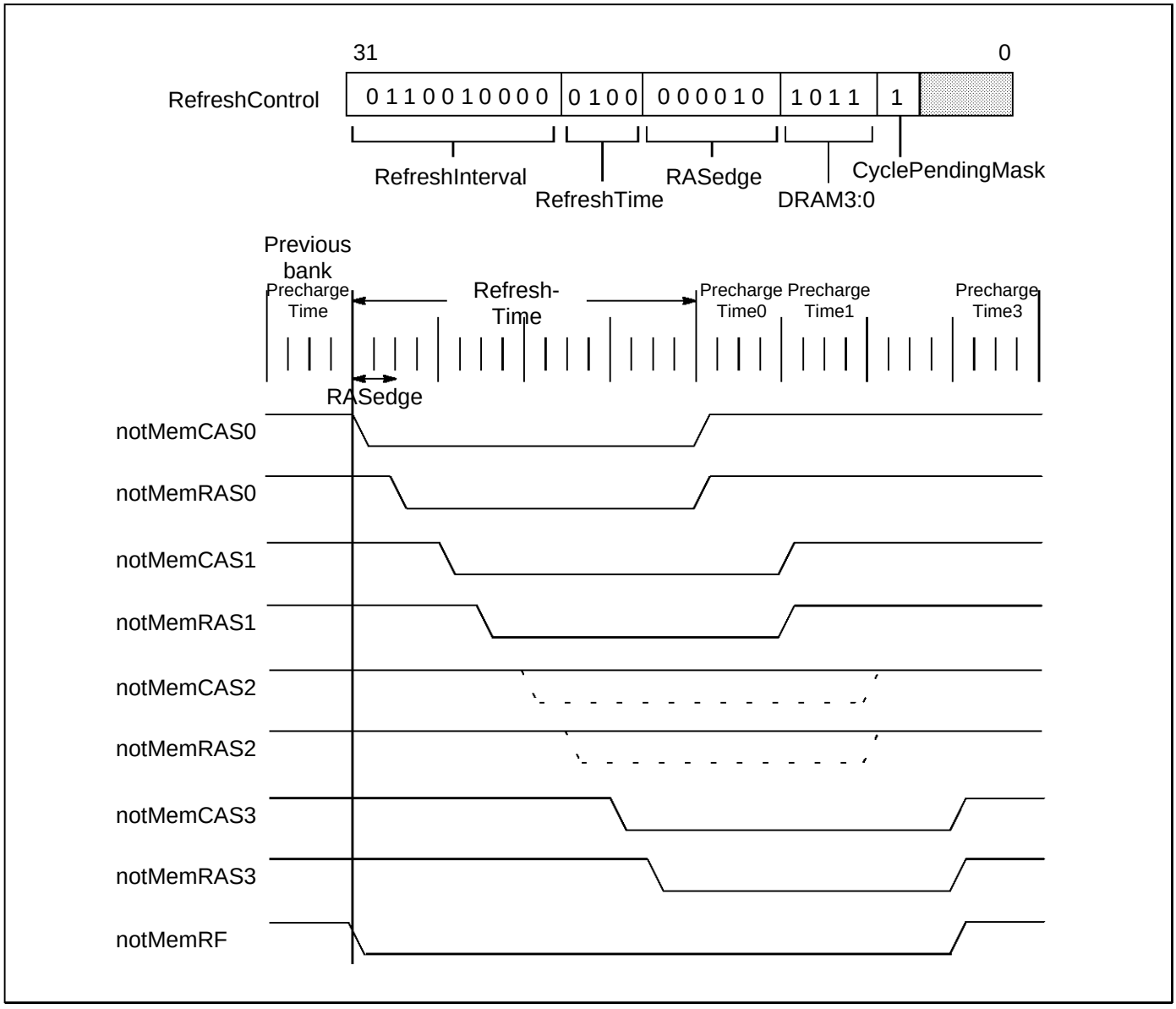


Figure 3.7 Programming of the refresh control register

3.4 Memory wait

The PMI is designed to synthesize the required waveforms from the parameters in the **TimingControl0-3** registers. However, external control can be provided if required. If the **WaitEnable** bit is disabled (set to 0) then the external cycles are controlled exclusively by the **TimingControl0-3** registers. If the **WaitEnable** bit is enabled (set to 1) then **MemWait** is defined to operate as follows:

- The **MemWait** pin is sampled during every clock cycle of the **RASTime** and the **CASTime** only. The sampling point is defined by t_{SVWV} and t_{SVWI} (see Table 3.3 and Figure 3.8).
- The action of **MemWait** is to suspend the state of the cycle counters and the level of the strobes from the end of the cycle in which it is sampled high. This is maintained as long as **MemWait** is asserted.
- When **MemWait** is deasserted counting continues as defined by the **TimingControl0-3** registers. Normal strobe behavior resumes from the end of the wait cycle during which **MemWait** is sampled low.
- If **MemWait** is asserted in the last cycle of a memory access then the results are undefined.

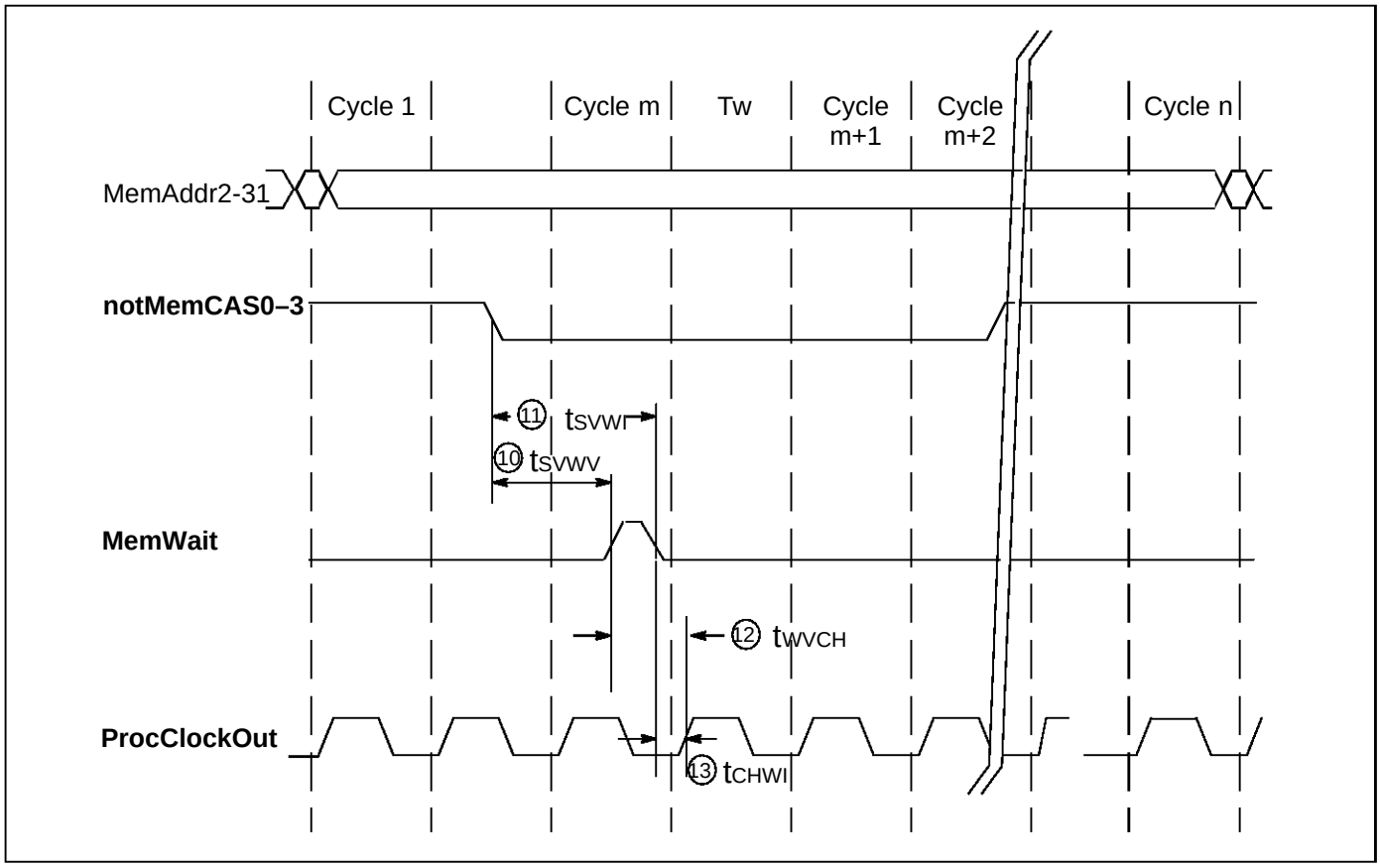


Figure 3.8 Memory wait timing

Symbol	No.	Parameter	Parameter type (see note 1)	Min	Nominal	Max	Units	Notes
t_{SVWV}	10	Wait setup time	nominal	–	(m∗4)–**E1Time**	–	phases	3,4
Dt_{SVWV}			skew	–	–	–19	ns	2
t_{SVWI}	11	Wait hold time	nominal	–	(m∗4)–**E1Time**	–	phases	3,4
Dt_{SVWI}			skew	+14	–	–	ns	2
t_{WVCH}	12	Wait valid before Clock	nominal	+17	–	–	ns	2
t_{CHWI}	13	Wait invalid after Clock	nominal	–5	–	–	ns	2

Table 3.3 Memory wait timings

Notes

1 *Parameter type*: refer to equation 1 in section 3.1.2 for an explanation of how t_n (nominal programmed value) and Dt_{SPEC} (the skew) are related.

2 The timings are based on the following loading conditions: address pin loaded with 25 pF and strobe pins loaded with 25 pF. All parameters that reference strobe, apply to *all* memory strobes e.g. **notMemWrB0-3**, **notMemRAS0-3**, **notMemCAS0-3**, **notMemPS0-3**.

3 A wait state will be inserted between cycle **m** and cycle **m+1** in an **n** cycle access if the specified relationship is met.

4 In an **n** cycle access a wait cycle cannot be added after cycle **n–1**. Also, a wait cycle cannot be added before cycle 1.

3.5 Booting from ROM

The IMS T9000 transputer can be bootstrapped from a ROM device, such as an EPROM or a Flash EPROM, or down control link (**CLink0**) from a host transputer or a computer with a link adaptor. In order to boot from ROM the **StartFromROM** pin must be held high.

3.5.1 Bootspace timing

The timing for accesses into the bootspace is not user programmable. The timing values used are defined in Figure 3.9. The timings have been deliberately relaxed to cover a wide range of ROM and T9000 speeds, typically 20 MHz to 30 MHz.

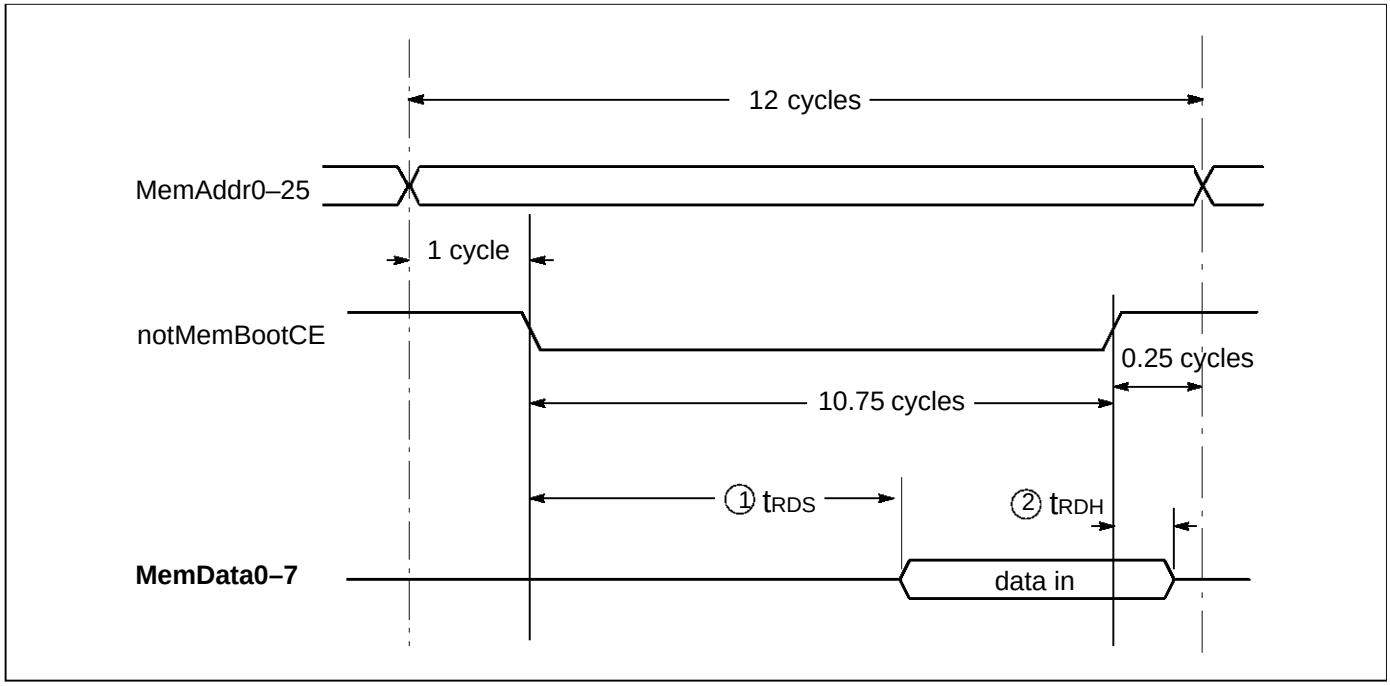


Figure 3.9 Boot cycle timing

Symbol	No.	Parameter	Parameter type (see note 1)	Min	Nominal	Max	Units	Notes
t_{RDS}	1	Read data valid after **notMemBootCE** low	nominal	–	44	–	phases	2
Dt_{RDS}			skew	–	–	–19	ns	
t_{RDH}	2	Read data hold after **notMemBootCE** high	nominal	–	1	–	phases	2
Dt_{RDH}			skew	–5	–	–	ns	

Table 3.4 Boot Cycle

Notes

1 *Parameter type*: refer to equation 1 in section 3.1.2 for an explanation of how t_n (nominal programmed value) and Dt_{SPEC} (the skew) are related.

2 Read data must be valid as specified in Table 3.1. These figures are irrespective of the programmed strobe edges as the T9000 subsystems latch data internally and so are not directly related to the programmed strobe timings.

3 The AC parameters of the strobe edges are equivalent to those defined for the strobes during a read/write cycle as shown in Table 3.1.

4 The equivalent Bus Release Time for the next boot bank is 5 cycles.

4 Events

The **EventIn0-3** and **EventOut0-3** pins provide an asynchronous handshake interface between external events and internal processes. Event channels provide process synchronization but cannot transfer any data. Each pair of **EventIn** and **EventOut** pins can act either as an input or an output event channel, but not both simultaneously.

Input event channel

When an external event takes an **EventIn** pin high the associated external event channel is made ready to communicate with a process. When both the event channel and the process are ready the processor takes the associated **EventOut** pin high and the process, if waiting, is scheduled. **EventOut** is removed after **EventIn** goes low. **EventIn** should not be taken low until **EventOut** has gone high.

Output event channel

The IMS T9000 asserts the **EventOut** pin to instruct external hardware to perform an action. When both the event channel and the external hardware are ready the external hardware asserts the associated **EventIn** pin and responds to the instruction. **EventIn** should be removed after **EventOut** goes low.[1]

Only one process may use each event channel at any given time. If no process requires an event to occur **EventOut** will never be taken high. **EventOut** is taken low when **Reset** occurs or when a *resetch* instruction is executed on that channel.

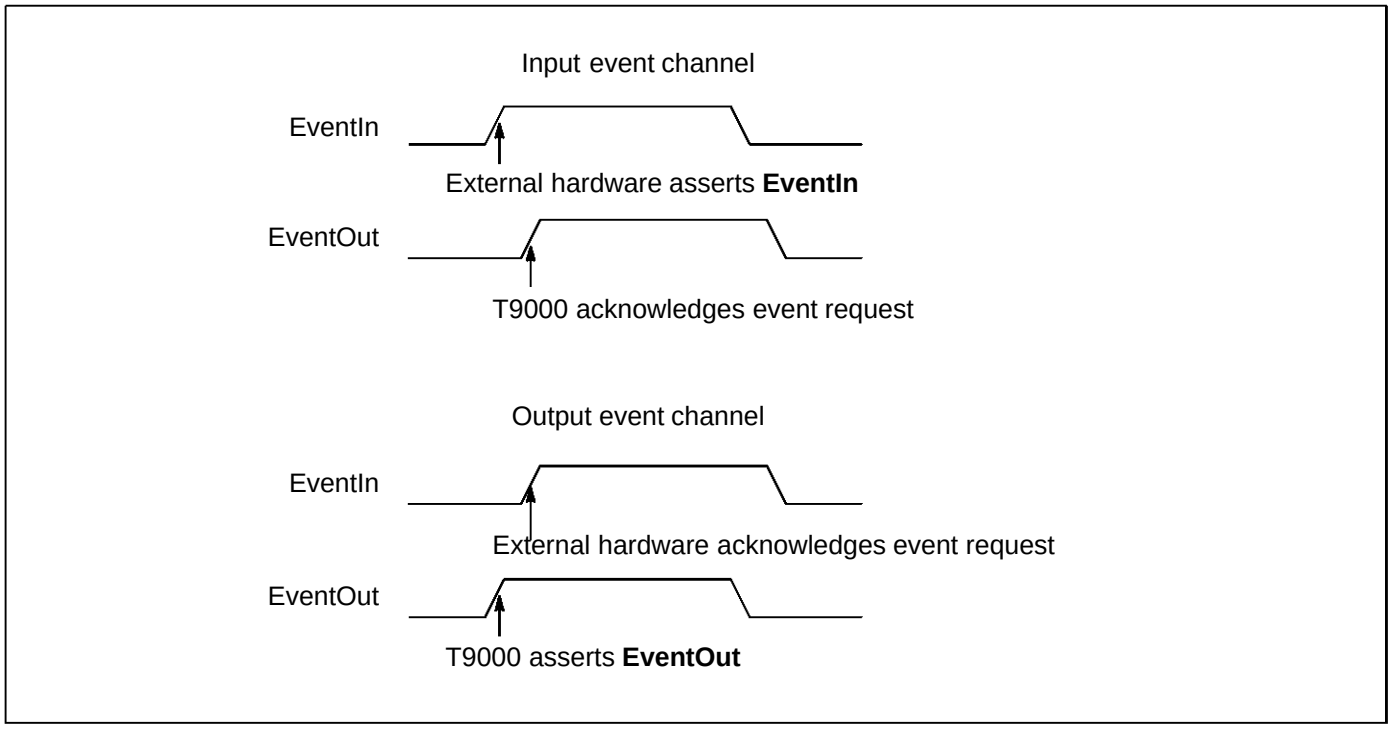


Figure 4.1 Event

Use of event channels with interrupts

An input event channel can be used for interrupts. Refer to *The T9000 Transputer Instruction Set Manual* for further information on how this can be achieved.

1 **EventIn** should not be set high until **EventOut** has been set high, and should not be removed until **EventOut** has gone low.

4.1 Event channel addresses

There are 8 words of memory reserved for event channels, from address #80000020 to #8000003C inclusive, see Figure 4.2. These addresses are also the channel addresses of the event channel. Each successive pair of words corresponds to one event channel. The lower address is used when the event is used for input, the higher address is used when the event is used for output. Thus the event channel address space is consistent with the virtual channel address space. In addition, provided the first event channel (**Event0**) is used for input, compatibility with the event channel address on the IMS T805 is achieved.

Each event channel must have a two word data structure to enable it to be used in resource mode. The (word-aligned) base of the block of memory for the resource mode words is pointed to by the **ExternalRCBase** configuration register. The two words for each of the four event channels are allocated at the bottom of the block.

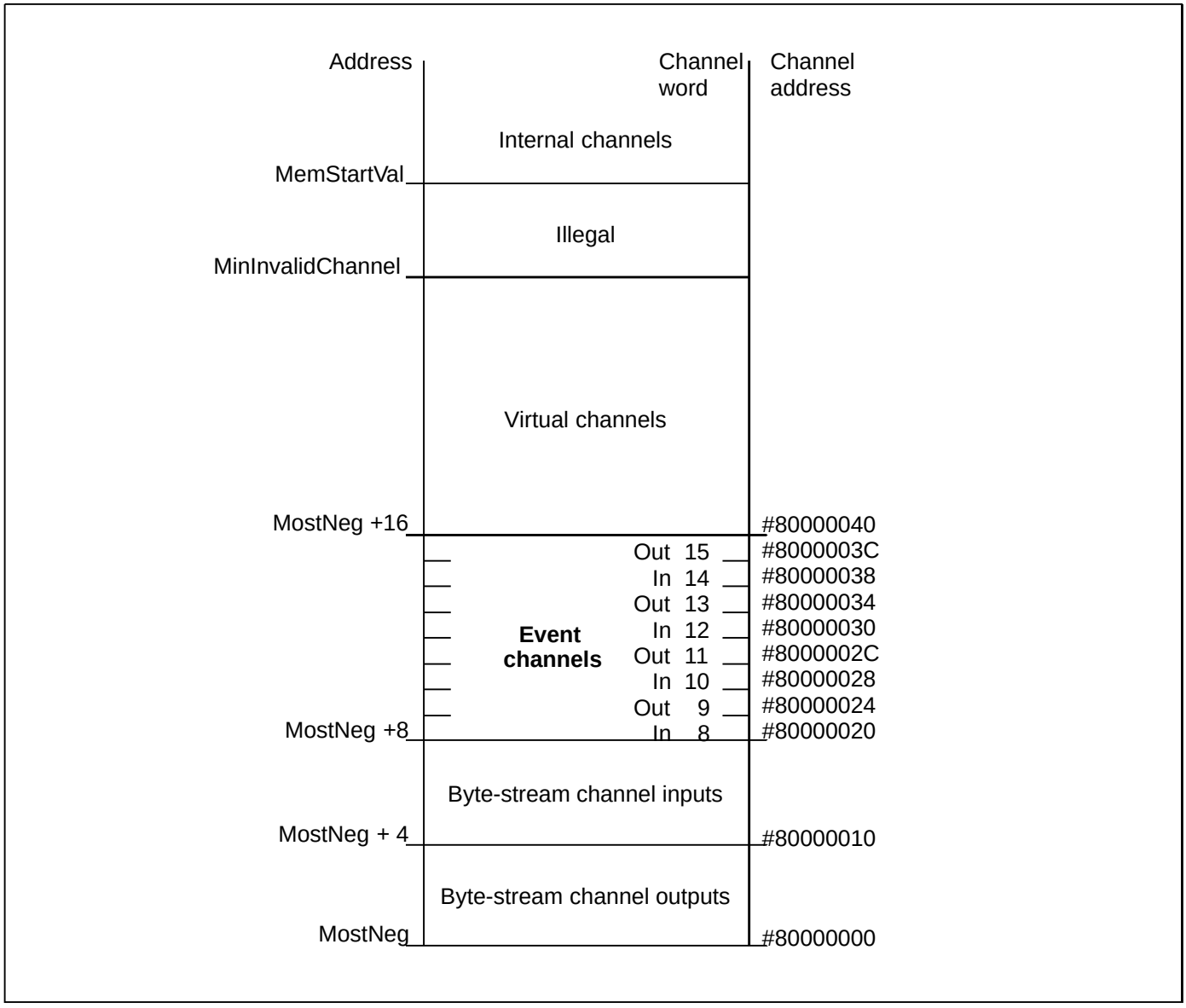


Figure 4.2 IMS T9000 channel address space

4.2 Event timing

Symbol	Parameter	Min	Nominal	Max	Units	Notes
tEIHEOH	**EventOut** response to **EventIn**	0	1		ns	
tEOHEIL	**EventIn** hold	0			ns	
tEILEOL	Delay before removal of **EventOut**	0			ns	
tEOLEIH	Delay before re-assertion of **EventIn**	1 **ProcClockOut**			ns	
tEOHEIH	Delay before assertion of **EventIn**	0			ns	
tEIHEOL	**EventOut** response to **EventIn**	0			ns	
tEOLEIL	Delay before removal of **EventIn**	0			ns	
tEILEOH	Delay before re-assertion of **EventOut**	0			ns	

Table 4.1 Event timing parameters

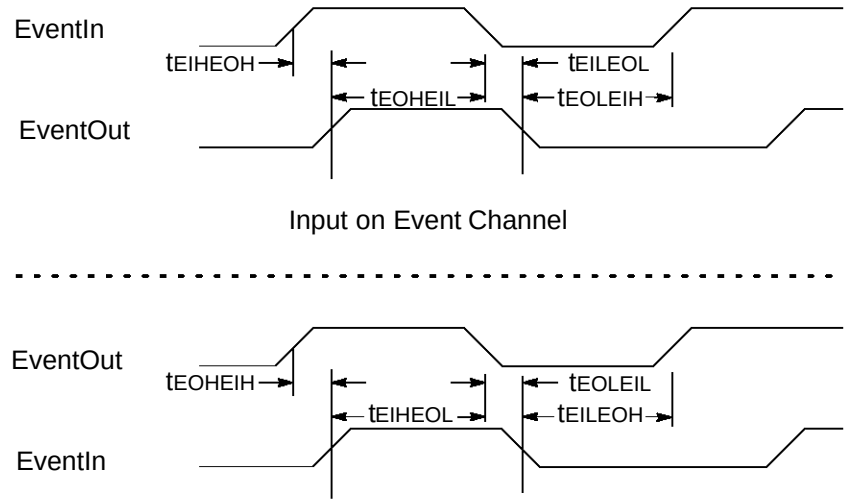


Figure 4.3 IMS T9000 event timing

5 Data/Strobe links

The IMS T9000 has four bidirectional links for normal inter-processor communications, and two additional links which can only be used for control purposes. All of these links use a protocol with two wires in each direction, one for data and one to carry a strobe signal, see Figure 5.1. These links are therefore referred to as data/strobe (DS-Links). The DS-Links are capable of:

- Up to 100 Mbits/s
- Unidirectional peak bandwidth of 10Mbytes/s per link
- Support for virtual channels and through routing.

The links are TTL voltage compatible and are optimized for driving a 100 ohm transmission lines. The links can be directly connected with no external buffering or other glue logic.

Figure 5.1 shows two transputers connected via DS-Links. In this example **Link0** of $T9000_1$ is connected to **Link3** of $T9000_2$.

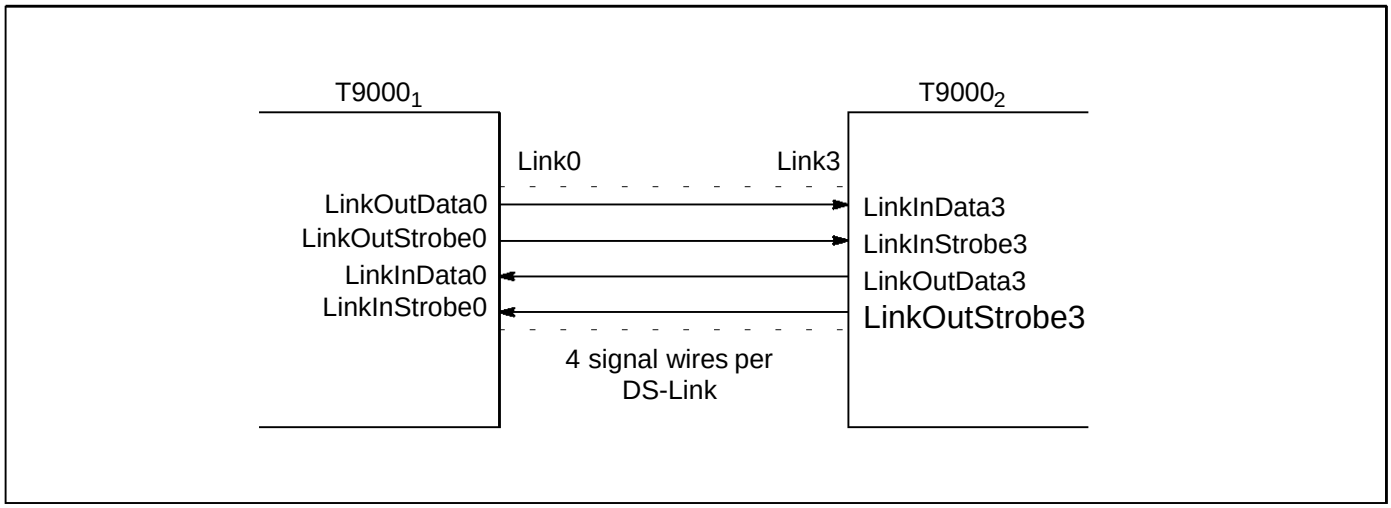


Figure 5.1 DS-Links

5.1 Link format and protocol

Each DS pair carries tokens and an encoded clock. The tokens can be data bytes or control tokens. Figure 5.2 shows the format of data and control tokens on the data and strobe wires. Data tokens are 10 bits long and contain a parity bit, a flag which is set to 0 to indicate a data token, and 8 bits of data. Control tokens are 4 bits long and contain a parity bit, a flag which is set to 1 to indicate a control token, and 2 bits to indicate the type of control token.

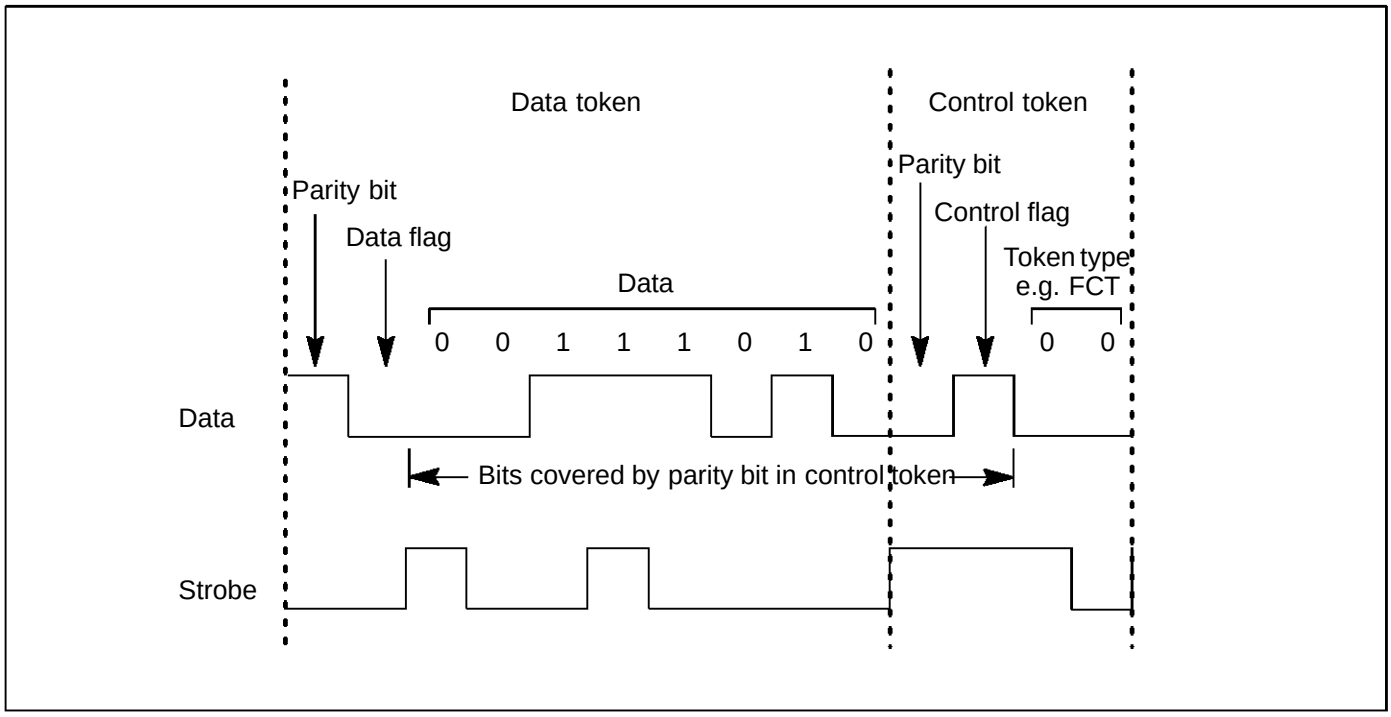


Figure 5.2 Link data and strobe formats

The DS-Link protocol ensures that only one of the two wires of the data strobe pair has an edge in each bit time. The levels on the data wire give the data bits transmitted. The strobe signal changes whenever the data signal does not. These two signals encode a clock together with the data bits, permitting asynchronous detection of the data at the receiving end.

The data and control tokens are of different lengths, for this reason the parity bit in any token covers the parity of the data or control bits in the previous token, and the data/control flag in the same token, as shown in Figure 5.2. This allows single bit errors in the token type flag to be detected. **Odd** parity checking is used. Thus the parity bit is set/unset to ensure that the bits covered, inclusive of the parity bit (see Figure 5.2), always contain an odd number of 1's. The coding of the tokens is shown in Table 5.1.

Token type	**Abbreviation**	**Coding**
Data token	–	P0DDDDDDDD
Flow control token	FCT	P100
End of packet	EOP	P101
End of message	EOM	P110
Escape token	ESC	P111
Null token	NUL	ESC P100

P = parity bit
D = data bit

Table 5.1 Token codings

One of the four control tokens is an escape token. The escape token is used to construct other 'composite' control tokens, see Table 5.1. One of these is the null token. Null tokens are sent in the absence of other tokens to ensure the immediate detection of parity errors and to enable link disconnection to be detected.

5.2 Link functional description

A link module consists of the units shown in Figure 5.3. The link control unit controls: link initialization, speed control, error reporting, etc. It connects to the link registers in the configuration space (refer to section 5.4). The link input unit interprets edge streams as tokens. The link output unit converts tokens to streams of edges.

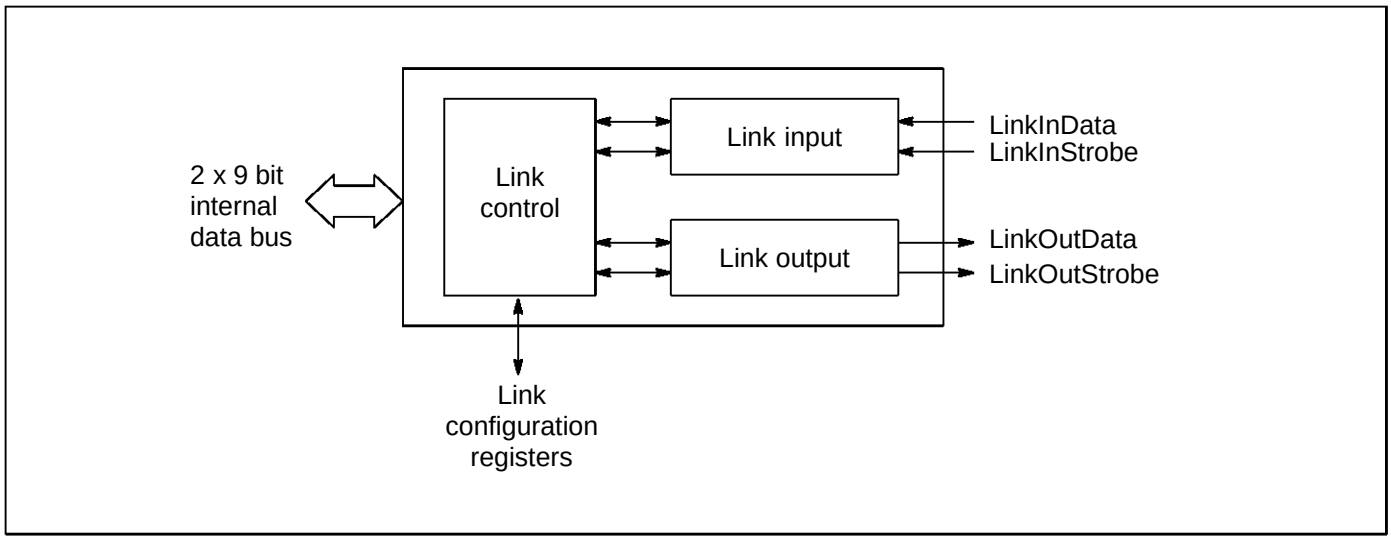


Figure 5.3 Link module

5.3 Link speed select

The IMS T9000 DS-Links support a range of communication speeds. The speed of a DS-Link is programmed by writing to registers in the configuration space.

Only the transmission speed of a DS-Link is programmed as reception is asynchronous. This means that DS-Links transmitting at different speeds can be connected, provided that each device is capable of receiving at the speed of the connected transmitter.

The transmission speed of all four DS-Links on the IMS T9000 are related to the speed of the 10 MHz base clock. This 10 MHz clock is multiplied by a programmable value to provide the root clock for all the DS-Links. The multiplication factor is programmed by writing to the **SpeedMultiply** bit in the **DSLinkPLL** register. This root clock is then optionally divided (by programming the **SpeedDivide** bits) by 1, 2, 4 or 8 independently for each DS-Link, giving a range of speeds. This arrangement allows each DS-Link to be run at one of four transmission speeds, as shown in Table 5.2.

SpeedMultiply	SpeedDivide1:0				BaseSpeed
	0:0	0:1	1:0	1:1	
	@1	@2	@4	@8	
8	80	40	20	10.0	10
10	100	50	25	12.5	10
12	Reserved	60	30	15.0	10
14	Reserved	70	35	17.5	10
16	Reserved	80	40	20.0	10
18	Reserved	90	45	22.5	10
20	Reserved	100	50	25.0	10

Table 5.2 DS-Link transmission speed in Mbits/sec

Note also that each DS-Link can be programmed to use a base rate clock of 10 MHz. At reset all DS-Links are configured to run at the **BaseSpeed** of 10 Mbits/sec. The **SpeedSelect** bit in the **Link0-3Mode** registers when set to 1 sets the respective DS-Link (**Link0-3**) to the speed selected by the **SpeedMultiply** and **SpeedDivide** bits, as opposed to the default base speed of 10 Mbits/s.

5.4 Link configuration registers

The DS-Links (in common with a number of other sub-systems of the IMS T9000) are controlled via a separate configuration address space. The registers in this address space are accessed via the *ldconf* and *stconf* instructions, or via *CPeek* and *CPoke* command messages received along **CLink0**.

Tables 5.3 to 5.7 describe the functionality of the DS-Links to be controlled, and the associated bit fields in the configuration registers. All SGS-THOMSON reserved bits should be set to 0.

Each DS-Link has four registers, the **LinkMode** register, **LinkCommand** register, **LinkStatus** register and **LinkWriteLock** register.

In addition the configuration space contains the **DSLinkPLL** register which contains the **SpeedMultiply** field. This determines the multiplication factor for the 10 MHz clock, to provide the root clock for all the DS-Links.

DSLinkPLL #1005		Read/Write
Bit	**Bit field**	**Function**
5:0	**SpeedMultiply**	Sets DS-Link master clock to required value (see Table 5.2). **Note**, 0 through to 7 are invalid values and should not be used.
31:6		SGS-THOMSON reserved.

Table 5.3 Bit fields in the **DSLinkPLL** register

The **Link0Mode**, **Link1Mode**, **Link2Mode**, **Link3Mode** registers (one for each of the four DS-Links) power up into a default state and may be re-programmed before or after the DS-Link has been started.

Note also that each DS-Link can be programmed to use a base rate clock of 10 MHz. At reset all DS-Links are configured to run at the **BaseSpeed** of 10 Mbits/sec. The **SpeedSelect** bit in the **Link0-3Mode** registers when set to 1 sets the respective DS-Link (**Link0-3**) to the speed selected by the **SpeedMultiply** and **SpeedDivide** bits, as opposed to the default base speed of 10 Mbits/s.

Link0-3Mode	#8001, #8101, #8201, #8301	Read/Write
Bit	**Bit field**	**Function**
1:0	**SpeedDivide**	The master link clock frequency is divided down by setting the **SpeedDivide** bits to obtain the transmission frequency for each DS-Link. Sets the transmit speed of the DS-Link (see Table 5.2). 00 = @1, 01 = @2, 10 = @4, 11 = @8
2	**SpeedSelect**	Sets the DS-Link to transmit at the speed determined by the **SpeedDivide** bits as opposed to the base speed of 10 Mbits/s.
3	**LocalizeError**	When set errors detected by the DS-Link are no longer reported to the control unit. Packets in transit at the time of an error will be discarded or truncated. (This bit is set by **Reset** to 1).
4	**1 (RESERVED)**	This bit should be written as 1.
5,7	**0 (RESERVED)**	These bits should be written as 0.
6	**Mute Input**	When set to 1, all transitions on the link input are ignored.
31:8		SGS-THOMSON reserved.

Table 5.4 Bit fields in the **Link0-3Mode** registers

The **Link0Command**, **Link1Command**, **Link2Command**, **Link3Command** registers are write only and contain four bits which when set cause a specific action to be taken by the DS-Link.

Link0-3Command	#8002, #8102, #8202, #8302	Write only
Bit	**Bit field**	**Function**
0	**ResetLink**	Resets the link engine of the **Link0-3**. The token state is reset, the flow control credit is set to zero, the buffers are marked as empty, and the parity state is reset. It also resets the **LinkStatus** register error bits.
1	**StartLink**	When a transition from 0 to 1 occurs **Link0-3** will be initialized and commence operation. It also resets the **LinkStatus** register error bits.
2	**ResetOutput**	Sets both Data and Strobe outputs of **Link0-3** low[1].
3	**WrongParity**	The **Link0-3** output will generate incorrect parity. This may be used to force a parity error on the transputer at the other end of the **Link0-3**.
31:4		SGS-THOMSON reserved.

Table 5.5 Bit fields in the **Link0-3Command** registers

1 Note that it is not necessary to do this in normal operation. This facility is provided in case the DS-Link is connected to non-transputer hardware which expects signals to be low after reset.

The **Link0Status**, **Link1Status**, **Link2Status**, **Link3Status** registers are read only and contain six bits which contain information about the state of the DS-Link.

Link0-3Status	**#8003, #8103, #8203, #8303**	**Read only**
Bit	**Bit field**	**Function**
0	**LinkError**	Flags that an error has occurred on the **Link0-3**.
1	**LinkStarted**	Flags that the output **Link0-3** has been started and no errors have been detected.
2	**ResetOutputComplete**	Flags that **ResetOutput** has completed on the **Link0-3**.
3	**ParityError**	Flags that a parity error has occurred on the **Link0-3**.
4	**DiscError**	Flags that a disconnect error has occurred on the **Link0-3**.
5	**TokenReceived**	Flags that a token has been seen on the **Link0-3** since **ResetLink** or **LinkError**.
31:6		SGS-THOMSON reserved.

Table 5.6 Bit fields in the **Link0-3Status** registers

In addition to the above mentioned registers each DS-Link has an associated **LinkWriteLock** register. The write lock register provides protection from writes by the processor, so that the link is guaranteed to function regardless of program behavior.

Setting the write lock register inhibits all configuration writes to this link from the CPU. All control link reset commands clear all write locks.

Note that the CPU can start and reset the links by means of *resetch* and *setchmode* instructions even if the write lock is set.

Link0-3WriteLock	**#8004,#8104,#8204,#8304**	**Read/Write**
Bit	**Bit field**	**Function**
0	**WriteLock**	When set to 1 it inhibits link configuration writes from the CPU.
31:1		SGS-THOMSON reserved.

Table 5.7 Bit fields in the **Link0-3WriteLock** registers

5.5 Initialization

5.5.1 Link state on start up

After reset all **LinkData** and **LinkStrobe** signals are low, without clocks. Following reset an initialization sequence sets the speed of the link clock. The DS-Links are initially inactive, with a default configuration. They are configured and started by configuration writes. Their status can be determined by configuration reads. Each DS-Link (**Link0-3**) must be explicitly started by writing to the **Link0-3Command** registers respectively. When a DS-Link is started up it transmits NUL tokens unless and until it receives a token. Once it has been started and received a token it sends two FCT's.

Data may not be transferred over the link until the receiving link has sent a FCT to signify that it has enough free buffer space to receive the data.

The receiving link receives and correctly decodes the tokens. However, only when the receiving link has been explicitly started by writing across the (internal) configuration bus can it send tokens back. NUL tokens are then sent until data is required.

5.5.2 Link state following reset

Both **LinkData** and **LinkStrobe** are low following reset to level 0 or level 1. The DS-Links output pins are unchanged after a reset to level 2. Note that a particular DS-Link can be explicitly reset via the configuration bus.

The control logic is responsible for resetting the link input and output following an error, however it does not reset the configuration registers, or the Data and Strobe outputs. These may all be reset independently via the configuration registers.

Physical links can be reset in one of the following ways:

- A *resetch* (reset channel) instruction whose channel parameter designates a byte-stream channel.
  This resets the queue registers for the link and resets and restarts the link.
- A *setchmode* (set channel mode) instruction with a parameter of 0, on a byte-stream channel, or by setting the **ResetLink** bit in the **Link0-3Command** configuration register via the configuration bus.
  The token state is reset, the flow control credit is set to zero, the buffers are marked as empty, and the parity state is reset.
- VCP global reset.
  This resets all four links.

The link automatically enforces a delay between reset and restart sufficient to guarantee that the other end will detect a disconnect error and complete its reset.

5.6 Link connections

DS-Links are not synchronized with **ClockIn** or **ProcClockOut** and are insensitive to their phases. Thus, links from independently clocked systems may communicate.

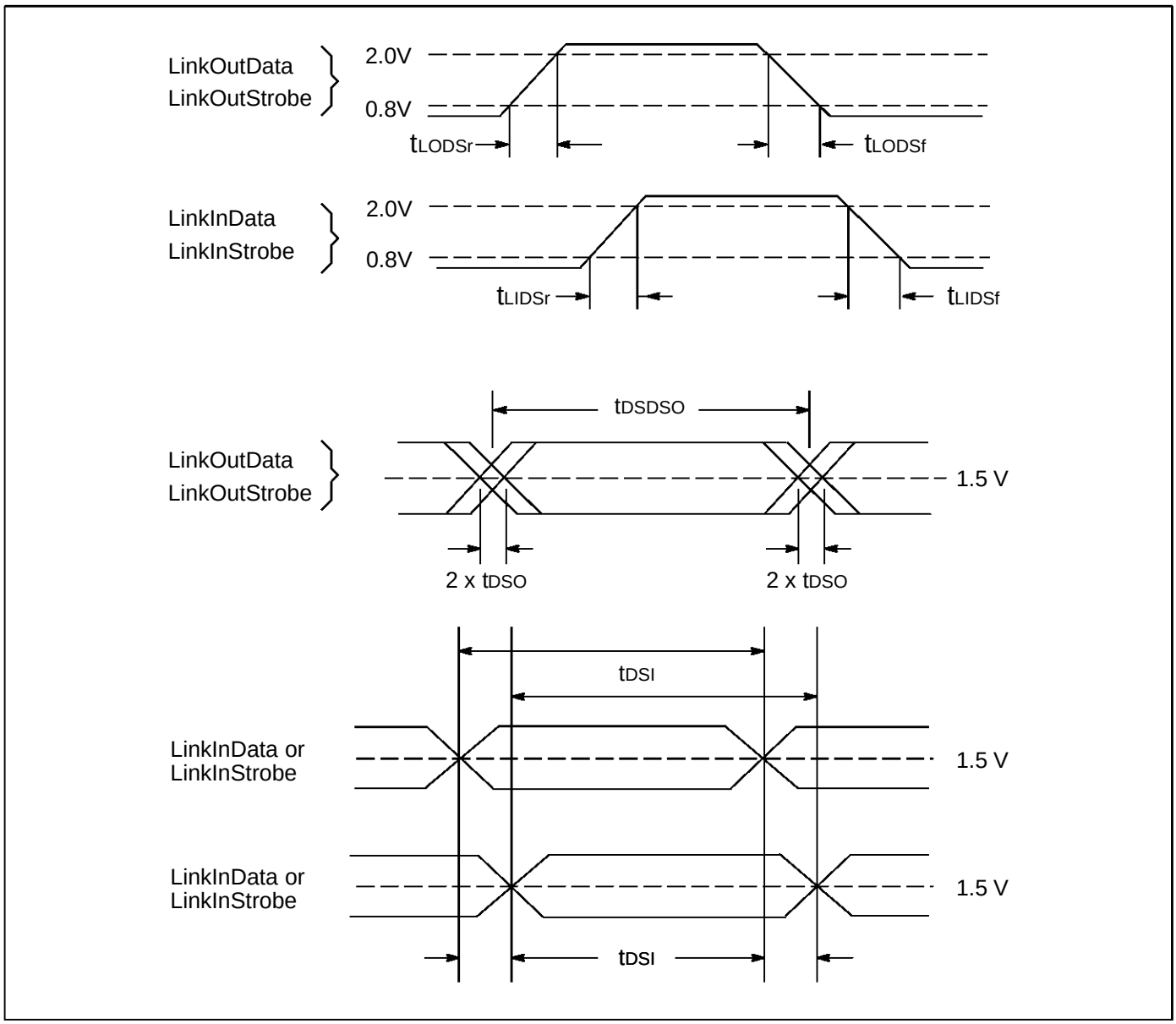


Figure 5.4 DS-Link timing

5.7 DS-Link parameters

Symbol	Parameter	Min	Nom	Max	Units	Notes
C_{LIZ}	LinkIn capacitance		7		pF	
t_{DSDSI}	Sustainable averaged input bit period	9		110	ns	
t_{DSDSO}	Output bit period	10		100	ns	
t_{DSI}	Data/strobe input edge minimum separation		2.5		ns	1,2,3
t_{DSO}	Data/strobe output skew			1	ns	4
t_{LIDSf}	LinkIn fall time (2.0–0.8V)			100	ns	6
t_{LIDSr}	LinkIn rise time (0.8–2.0V)			100	ns	6
t_{LODSf}	LinkOut fall time (2.0–0.8V)			7	ns	7
t_{LODSr}	LinkOut rise time (0.8–2.0V)			7	ns	7
R_{OH}	Output impedance (output driving high)	110		247	Ω	8
R_{OL}	Output impedance (output driving low)	63		104	Ω	8

Table 5.8 DS-Link timings

Notes

1 t_{DSDSO} represents the minimum and maximum programmable bit periods.

2 t_{DSI} is the shortest permissible spacing of 2 consecutive edges on the Data and Strobe wires (1 edge of either sense on each wire). If arriving Data and Strobe edges are skewed to the extent that this parameter is exceeded then the order of the edges becomes ambiguous and a parity error is likely to result.

3 Edge separation includes consecutive edges of a data input or a strobe input.

4 Based on a slew rate of 1.5 V/s, monotonic across the transition region. For other values of slew rate, use the following formula:

$$1.0 + (k * \text{slew rate}) \text{ where } k=1.0$$

5 t_{DSO} is the maximum discrepancy between the time when a DS Output edge (either sense) starts a transition and the theoretical ideal (i.e. all consecutive DS edges spaced by t_{DSDSO}).

6 Edges must be monotonic, hence faster edges are recommended unless the link is to be used in a noise free environment.

7 Measurement based on a loading of 25pF.

8 The link output drivers have been optimized for driving a 100Ω transmission line.

5.7.1 Link Input and Output relative skews

For the skew parameters to be valid for a wide range of operating speeds (10 – 100 Mbits/s) certain parameters must be made relative to edge rates, as the interaction of edge rates and logic threshold have significant impact on the skew. Note that skew is measured relative to the edges crossing a nominal 1.5V logic threshold.

t_{DSI} = *Fixed skew* + k * (the larger of t_{LIDSr} and t_{LIDSf})

Where *Fixed Skew* is related to the worst case DSDecoder input skew rejection and internal input path mismatches, and *k* is found by characterization and related to minimum variation in input threshold and input pad propagation delay.

t_{DSO} = *Fixed skew*

where: *Fixed Skew* is related to the worst case Link Output PLL jitter and internal output path mismatch.

5.7.2 Skew budget

The concept here is that in order to eliminate the risk of DSLink parity errors due to the relative skew between Data and Strobe inputs a system designer must ensure that the sum of $2t_{DSO}$ and the relative skew between Data and Strobe induced by all system interconnect and buffering must be less than $t_{DSDSO} - t_{DSI}$.

Note that an edge rate dependent calculation must be performed for external buffers with variable thresholds in order to calculate worst case $t_{EXTSkew}$ for both Data and Strobe, i.e. :

$$2t_{DSO} + t_{EXTSkew} < t_{DSDSO} - t_{DSI}$$

The parameter t_{DSO} on the left hand side of the expression is multiplied by two to allow for the worst case situation of Data and Strobe undergoing maximum skew in opposite directions.

6 Clocking phase locked loops

Two on-chip phase locked loops (PLL) generate all the internal high frequency clocks from a single clock input, simplifying system design and avoiding problems of distributing high speed clocks externally. This chapter details the PLL input specifications, decoupling requirements and speed selections.

There is one PLL for the system clocks and one for the link clocks. Each PLL has six outputs, four quad phase signals and two bi-phase signals. The global system clocks use the four quad phase signals from the system clock PLL. The link clock is one of the bi-phase 100 MHz clocks from the link PLL.

6.1 PLL decoupling

The PLL's require a decoupled power supply for satisfactory operation. The decoupling is performed externally by connecting a 1mF ceramic capacitor between the **CapPlus** and **CapMinus** pins on the chip. A surface mounted ceramic capacitor with an ESR (Equivalent Series Resistance) of less than 3 ohms should be used. In order to keep stray inductances low, the total PCB track length should be less than 20 mm, thus the capacitor should be no more than 10 mm from the chip. The connections must not touch power supplies or other noise sources.

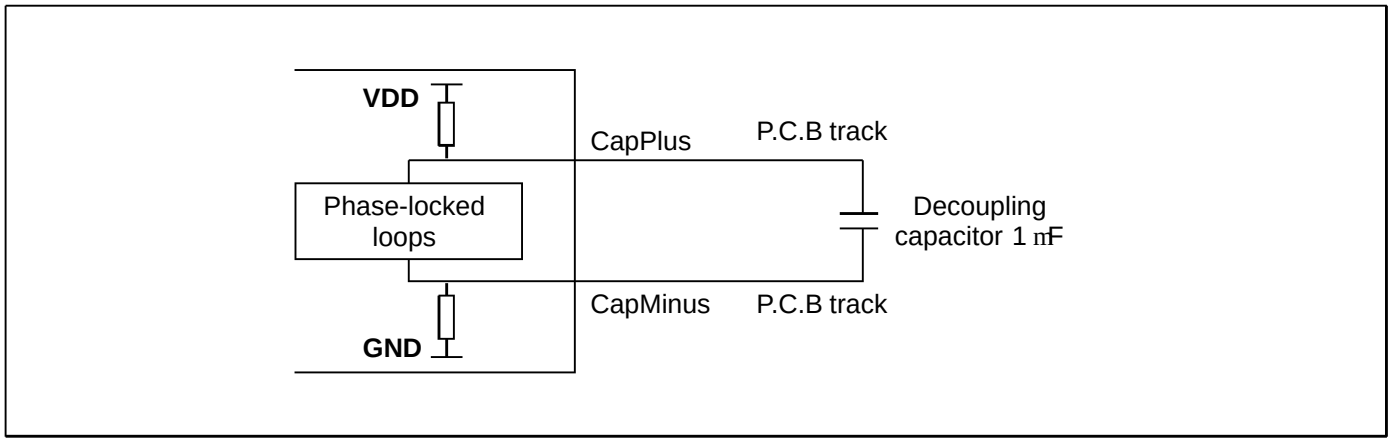


Figure 6.1 Recommended PLL decoupling

6.2 Clock input

The high frequency internal clocks are derived from the clock frequency supplied by the user. The user supplies the clock frequency for input to the PLL's via the **ClockIn** input. The nominal frequency of this clock for all transputer family components is 5 MHz, regardless of device type, transputer word length or processor cycle time.

A number of transputer devices may be connected to a common clock, or may have individual clocks providing each one meets the specified stability criteria. In a multi-clock system the relative phasing of **ClockIn** clocks is not important, due to the asynchronous nature of the links. Mark/space ratio is unimportant provided the specified limits of **ClockIn** pulse widths are met.

Oscillator stability is important. **ClockIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **ClockIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

The timing requirements for **ClockIn** are given in section 6.3.

6.3 ClockIn timings

Symbol	Parameter	Min	Nom	Max	Units	Notes
t_{DCLDCH}	**ClockIn** pulse width low	40			ns	
t_{DCHDCL}	**ClockIn** pulse width high	40			ns	
t_{DCLDCL}	**ClockIn** period		200		ns	1, 2
t_{DCr}	**ClockIn** rise time			10	ns	3
t_{DCf}	**ClockIn** fall time			8	ns	3

Table 6.1 **ClockIn** timings

Notes

1 Measured between corresponding points on consecutive falling edges.

2 This value allows the use of 200 ppm crystal oscillators for two devices connected together by a link.

3 Clock transitions must be monotonic within the range V_{IH} to V_{IL} (refer to Electrical specifications chapter).

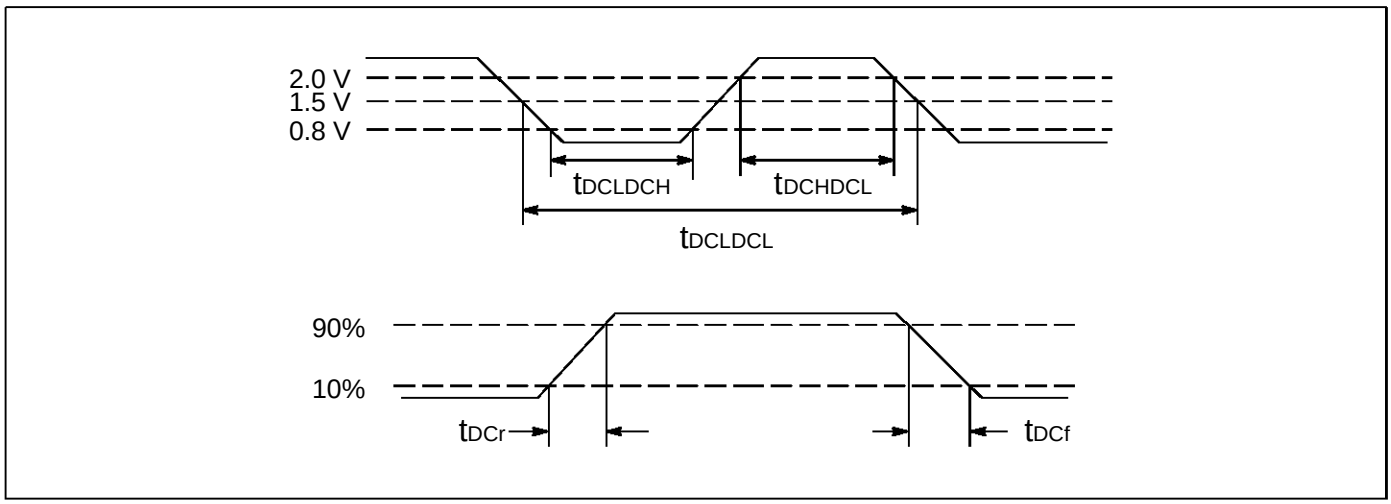


Figure 6.2 **ClockIn** timing

6.4 Processor speed selection

The processor internal clock rate is variable in discrete steps. The clock rate at which the IMS T9000 runs at is determined by the logic levels applied on the three speed select lines **ProcSpeedSelect0-2** as detailed in Table 6.2. Note that the processor cycle time given in Table 6.2 is a nominal value; it can be calculated more accurately using the phase lock loop factor **PLLx** (see section 6.5 below).

ProcSpeed Select2	ProcSpeed Select1	ProcSpeed Select0	Processor clock speed MHz	Processor cycle time ns	Phase lock loop factor (PLLx)
1	1	0	20	50.0	4.0
1	1	1	25	40.0	5.0
0	0	0	30	33.3	6.0

Table 6.2 Processor speed selection

6.5 Processor clock output

The processor output clock (supplied on the **ProcClockOut** output) is derived from the internal processor clock, which is in turn derived from **ClockIn**. It provides an output timing signal at the rated clock frequency of the device. Its period is equal to one internal microcode cycle time, and can be derived from the formula:

$$t_{DCLDCL} = t_{DCLDCL} / PLLx$$

where: t_{PCLPCL} is the **ProcClockOut Period**, t_{DCLDCL} is the **ClockIn Period** and **PLLx** is the phase lock loop factor for the relevant speed part.

6.6 ProcClockOut timings

Symbol	Parameter	Min	Nom	Max	Units	Notes
t_{PCLPCL}	**ProcClockOut** period		–		ns	1
t_{PCHPCL}	**ProcClockOut** pulse width high		$\frac{t_{PCLPCL}}{2}$		ns	
Dt_{PCHPCL}	**ProcClockOut** pulse width high	–2.5	–	+2.5	ns	
t_{PCLPCH}	**ProcClockOut** pulse width low		$\frac{t_{PCLPCL}}{2}$		ns	
Dt_{PCLPCH}	**ProcClockOut** pulse width low	–2.5	–	+2.5	ns	

Table 6.3 **ProcClockOut** timings

Notes

1 Nominal value dependent upon processor speed selection (see section 6.5)

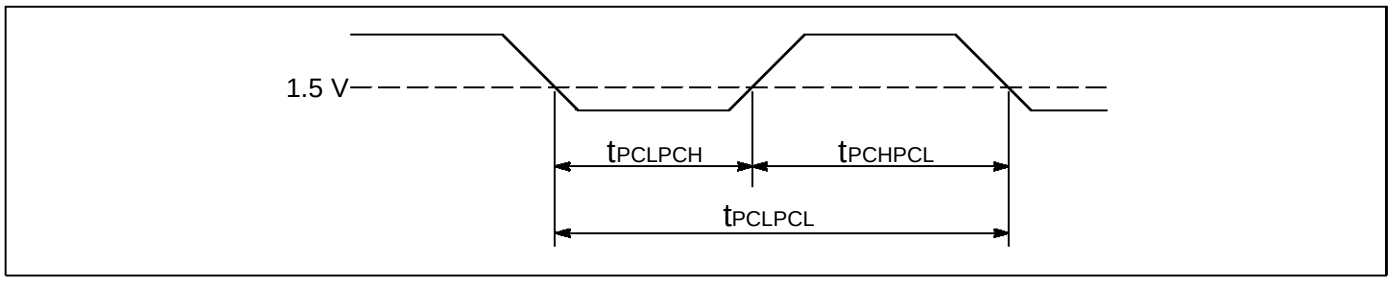


Figure 6.3 **ProcClockOut** timing

6.7 ProcClockOut stability

The following table shows how the variation in ProcClockOut period stability varies against Proc-ClockOut period. This parameter must be taken into account when calculating absolute PMI timing characteristics for specific PMI configurations. Refer to section 3.1.2 *AC timing characteristics* to see how this value is used.

Symbol	Parameter	Units				Note
t_{PCLPCL}	period	ns	50	40	33.3	
t_{PCstab}	stability	%	2	2	2.0	1

Table 6.4 **ProcClockOut** stability value against clock period

Notes

1 Stability is the variation of cycle periods between two consecutive cycles, measured at corresponding points on the cycles.

7 Static signals

7.1 Timing for static signals

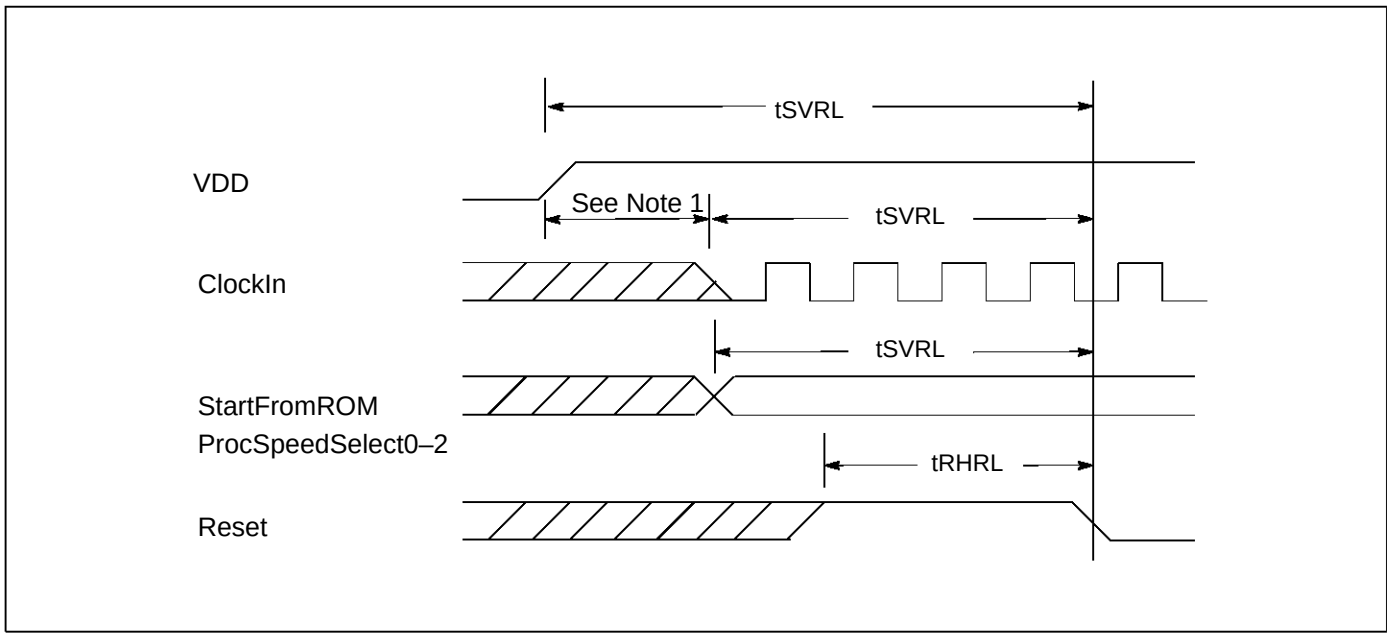


Figure 7.1 Timing for static signals

Symbol	Parameter	Minimum (ms)	Note
t_{SVRL}	Signal valid to Reset low	20	
t_{RHRL}	Reset high to Reset low	10	

Notes

1 The T9000 may dissipate more power when **ClockIn** is not running than in normal operation.

8 Electrical specifications

Inputs and outputs are TTL compatible.

8.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Units	Notes
VDD	DC supply voltage	0	7.0	V	1,2,3,4,5
V_I, V_O	Voltage on input and output pins	–0.5	VDD+0.5	V	1,3,4,5
I_I	Input current		+10	uA	6
t_{OSC}	Output short circuit time (one pin)		1	s	4
T_S	Storage temperature	–65	150	_C	4

Table 8.1 Absolute maximum ratings

Notes

1 All voltages are with respect to **GND**.

2 Power is supplied to the device via the **VDD** and **GND** pins. Several of each are provided to minimize inductance within the package. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100 nF low inductance (e.g. ceramic) capacitor between **VDD** and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

3 Input voltages must not exceed specification with respect to **VDD** and **GND**, even during power-up and power-down ramping, otherwise *latchup* can occur. CMOS devices can be permanently damaged by excessive periods of latchup.

4 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Unused inputs should be tied to an appropriate logic level such as **VDD** or **GND**.

6 The input current applies to any input or output pin and applies when the voltage on the pin is between **GND** and **VDD**.

8.2 Operating conditions

Symbol	Parameter	Min	Max	Units	Notes
VDD	DC supply voltage	4.75	5.25	V	1
V_I, V_O	Input or output voltage	0	VDD	V	1,2
C_L	Load capacitance on any pin			pF	3
T_A	Operating temperature range	0	TA_{MAX}	_C	4

Table 8.2 Operating conditions

Notes

1 All voltages are with respect to **GND**.

2 Excursions beyond the supplies are permitted but not recommended.

3 Maximum capacitance per address/ strobe/ data pin given in Table 8.4.

4 For details of T_{AMAX}, refer to chapter 9.

8.3 DC characteristics

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
V_{IH}	High level input voltage		2.0	VDD+0.5	V	1,2
V_{IL}	Low level input voltage		–0.5	0.8	V	1,2
I_I	Input current	@ GND<VI<VDD		10	mA	1,2
V_{OH}	Output high voltage	@ IOH=2mA	VDD–2		V	1,2,4
V_{OL}	Output low voltage	@ IOL=4mA		0.4	V	1,2,4
I_{OZ}	Tristate output current	@ GND<V0<VDD		10	mA	1,2
P_D	Power dissipation			4.0	W	2,3
C_{IN}	Input capacitance	@ f=1MHz		7	pF	
C_{OZ}	Output capacitance	@ f=1MHz		10	pF	

Table 8.3 DC characteristics

Notes

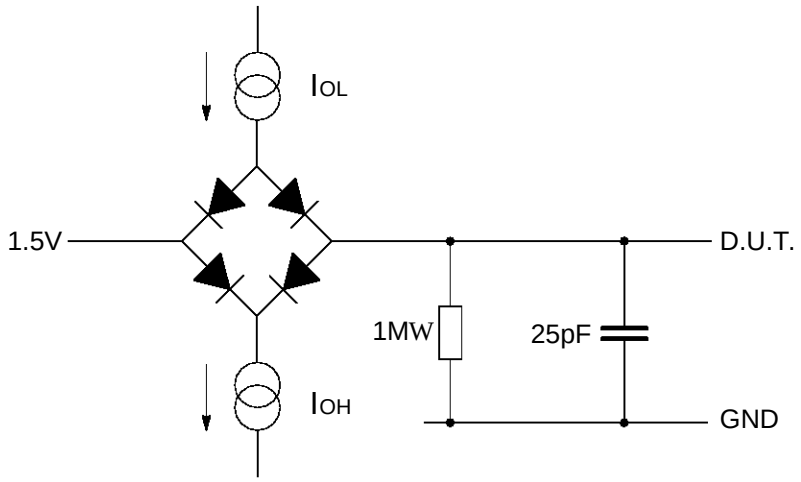
1 All voltages are with respect to **GND**.

2 Parameters for IMS T9000 measured at 4.75V<**VDD**<5.25V and 0^{o}C<**TA**<T_{AMAX}.
Input clock frequency = 5 MHz.

3 Power dissipation varies with output loading and program execution.
Power dissipation for processor operating at 20 MHz with 25pF loading.
Power dissipation increases with clock speed.

4 For link outputs, IOH=1mA, IOL=1mA.

8.4 Equivalent circuits



Note: This circuit represents the device sinking IOL and sourcing IOH with a 25pF capacitive load.

Figure 8.1 Load circuit for AC measurements

Notes

1 IOL=IOH=0mA except for certain AC parameters (Data bus, Address Bus, Strobes, t_{AZMGH}, t_{DZMGH}, t_{SZMGH}, t_{MGLAV}, t_{MGLDV},t_{MGLSV}) when IOL and IOH have the values stated in Table 8.3.

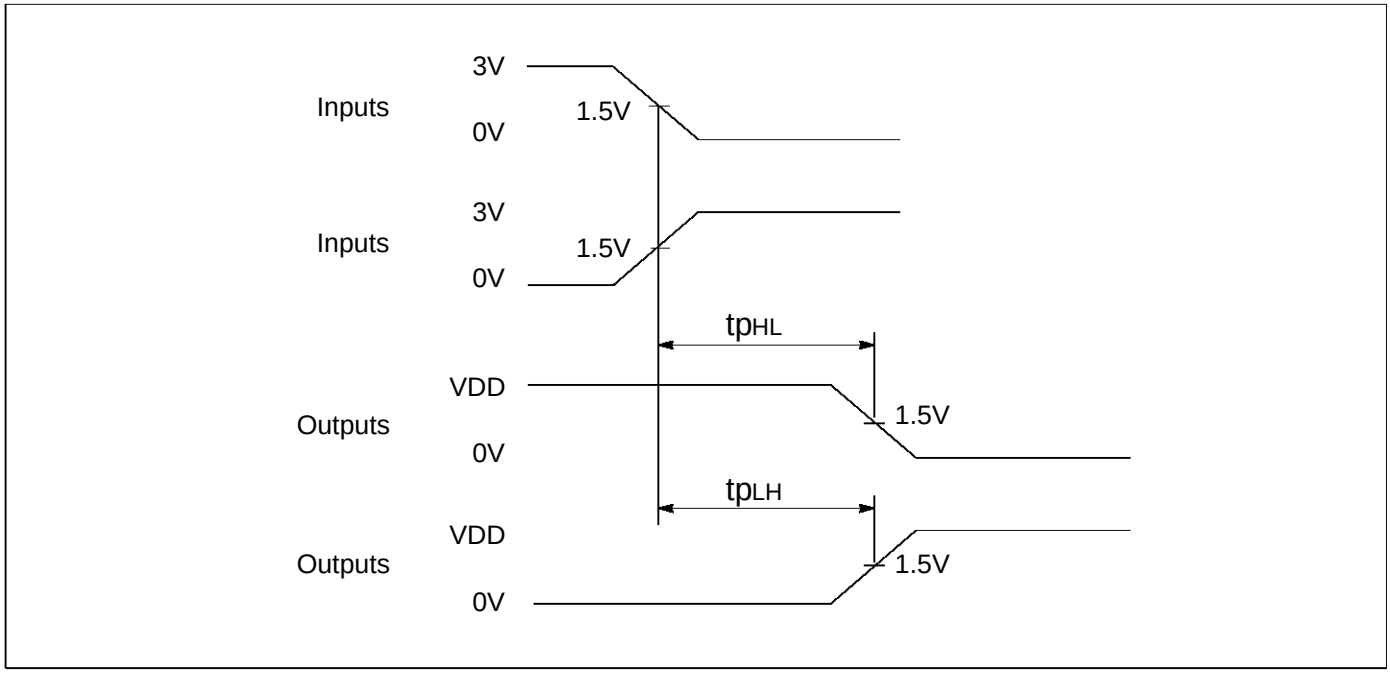


Figure 8.2 AC measurements timing waveforms

8.5 Power rating

The internal power dissipation of the IMS T9000 depends on **VDD**, as shown in Figure 8.3, and is substantially independent of temperature. It is dependent on operating frequency and program execution. The typical internal power dissipation (P_{INT}) for an IMS T9000 operating at 20 MHz is 3.0W (see Figure 8.3).

The total power dissipation of the IMS T9000 is dependent on operating frequency, program execution, external memory configuration, and output pin loading.

The total peak power dissipation P_D of the chip is:

$$P_D = P_{INT} + P_{PMI}$$

The peak power dissipation of the PMI (P_{PMI}) can be determined for a given memory configuration from the following equation:

$$P_{PMI} = VDD^2 \quad ((n_{pA} \quad C_{pinA} \quad f_A) + (n_{pS} \quad C_{pinS} \quad f_S) + (n_{pD} \quad C_{pinD} \quad f_D))$$

where:

n_p is the total number of active (address/ strobe/ data) pins
C_{pin} is the actual capacitance per (address/ strobe/ data) pin
f is the effective operating frequency per (address/ strobe/ data) pin

The maximum allowable capacitances that can be connected to each class of pins are shown in Table 8.4.

Symbol	Parameter	Max	Units
C_{pinA}	Capacitance per address pin	250	pF
C_{pinS}	Capacitance per strobe pin	60	pF
C_{pinD}	Capacitance per data pin	60	pF
n_{pA} C_{pinA}	Total address bus capacitance	2500	pF
n_{pS} C_{pinS}	Total strobe pins capacitance	500	pF
n_{pD} C_{pinD}	Total data bus capacitance	5000	pF

Table 8.4 Capacitance specifications

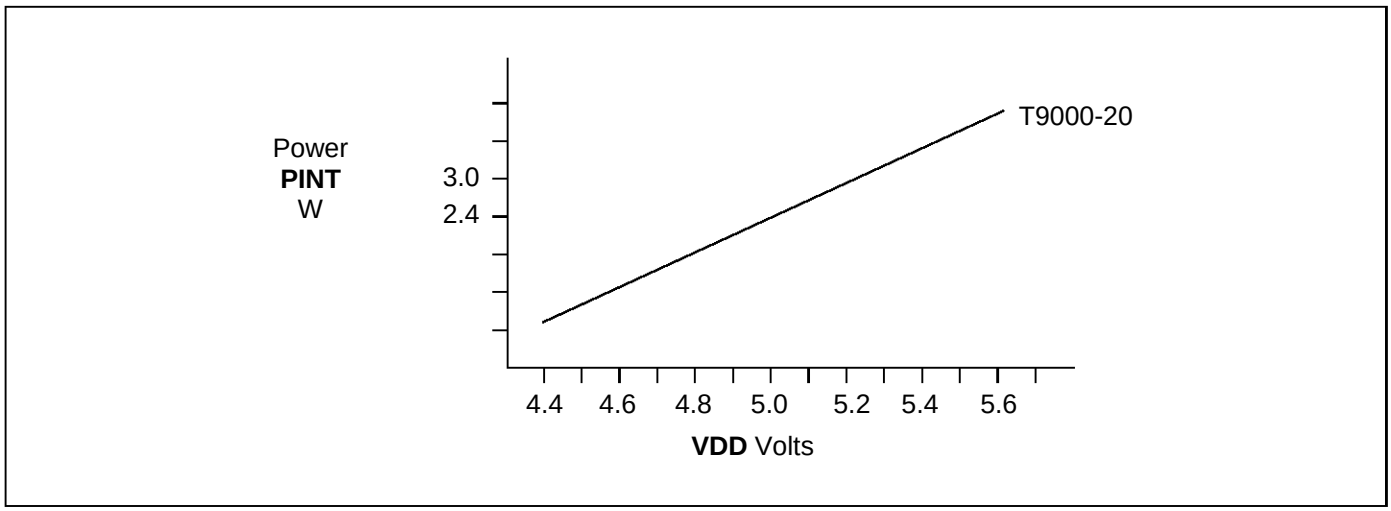


Figure 8.3 Internal power dissipation vs VDD

9 Thermal data

The IMS T9000 is tested to a maximum silicon junction temperature of 100_C. For operation within the given specifications, the case temperature should not exceed 95_C.

Given a maximum operating junction temperature of 100_C, the following maximum power conditions apply:

Conditions	Maximum Power (Watts)
Still air at 30_C	3.41
Case held at 95_C	15.0

For actual maximum power dissipation see section 8.3.

For temperatures above 100_C the operation of the device cannot be guaranteed and reliability may be impaired.

For further information on reliability refer to the SGS-THOMSON Microelectronics Quality and Reliability Program.

External thermal management must be used to ensure optimum performance and reliability.

10 Package specifications

The IMS T9000 is available in a 208 pin ceramic leaded chip carrier (CLCC) package. It is intended for cavity down assembly. The dimensions and thermal characteristics detailed below apply to cavity down installation.

10.1 208 pin CLCC package pinout

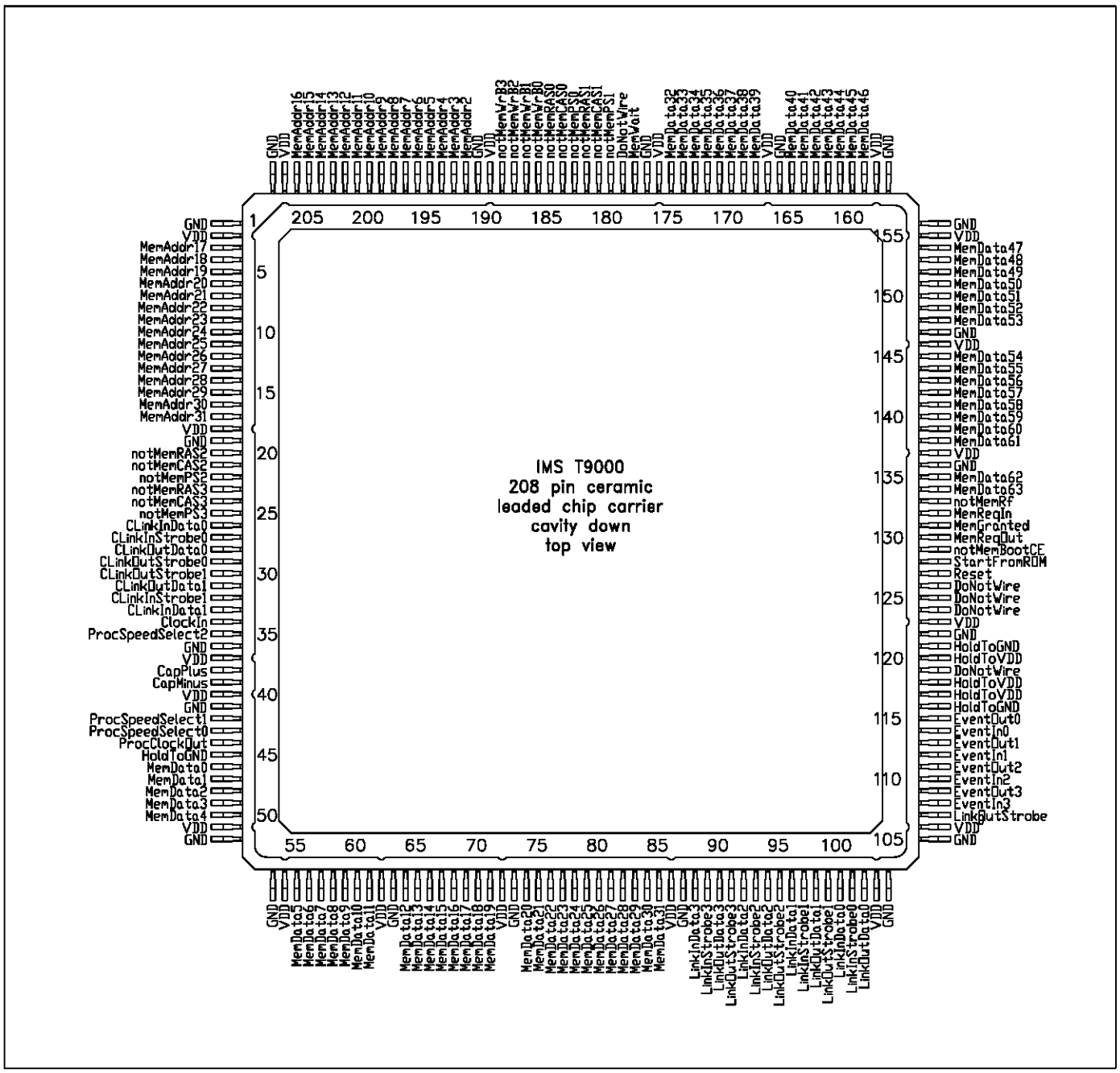
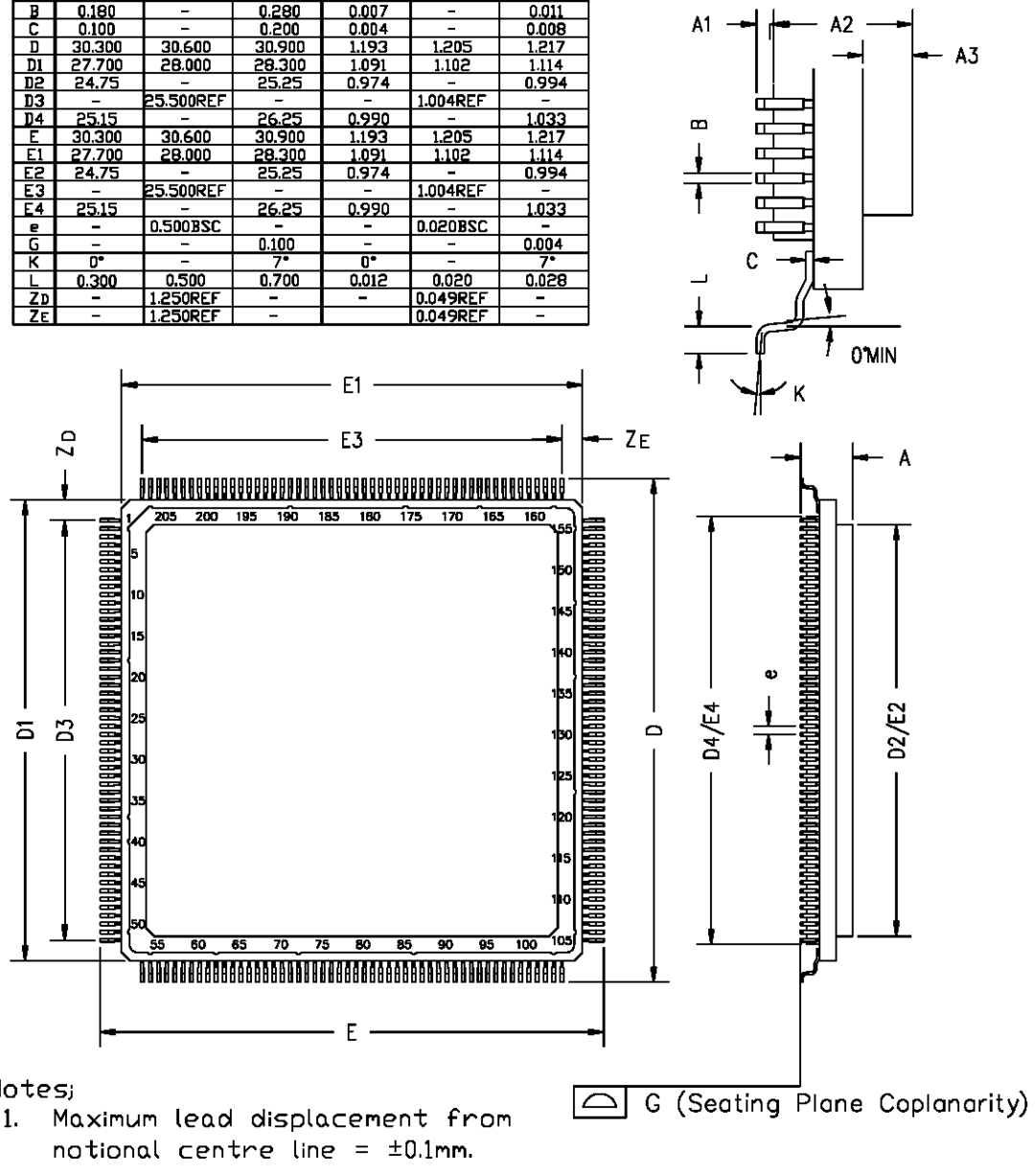


Figure 10.1 208 pin CLCC package pinout

10.2 208 pin CLCC package dimensions

DIM	CONTROL DIMENSIONS mm			ALTERNATIVE DIMENSIONS INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	3.500	–	–	0.138
A1	0.25	–	–	0.010	–	–
A2	2.33	2.63	2.93	0.092	0.104	0.115
A3	–	–	1.000	–	–	0.039
B	0.180	–	0.280	0.007	–	0.011
C	0.100	–	0.200	0.004	–	0.008
D	30.300	30.600	30.900	1.193	1.205	1.217
D1	27.700	28.000	28.300	1.091	1.102	1.114
D2	24.75	–	25.25	0.974	–	0.994
D3	–	25.500REF	–	–	1.004REF	–
D4	25.15	–	26.25	0.990	–	1.033
E	30.300	30.600	30.900	1.193	1.205	1.217
E1	27.700	28.000	28.300	1.091	1.102	1.114
E2	24.75	–	25.25	0.974	–	0.994
E3	–	25.500REF	–	–	1.004REF	–
E4	25.15	–	26.25	0.990	–	1.033
e	–	0.500BSC	–	–	0.020BSC	–
G	–	–	0.100	–	–	0.004
K	0°	–	7°	0°	–	7°
L	0.300	0.500	0.700	0.012	0.020	0.028
ZD	–	1.250REF	–	–	0.049REF	–
ZE	–	1.250REF	–		0.049REF	–



Notes;
1. Maximum lead displacement from notional centre line = ±0.1mm.

Figure 10.2 208 pin CLCC package dimensions

10.3 208 pin CLCC package thermal characteristics

The junction to case thermal resistance (q_{JC}) of the package is given below. Information on thermal management of the IMS T9000 is given in chapter 9.

Symbol	Parameter	Min	Nom	Max	Units
q_{JC}	Junction to case thermal resistance			1	_C/W

Table 10.1 Thermal resistance

11 Ordering

This section indicates the designation of speed and package selections for the various devices. Speed of **ClockIn** is 5 MHz for all parts. Transputer processor cycle time is nominal; it can be calculated more exactly using the phase lock loop factor **PLLx**, as detailed in the programmable memory section.

For availability contact your local SGS-THOMSON sales office or authorized distributor.

SGS-THOMSON designation	Processor clock speed	Processor cycle time	PLLx	Package
IMST900-F20S	20.0	50	4.0	208 pin CLCC

Table 11.1 IMS T9000 ordering details