1 Upgrading INMOS evaluation boards to take T800's

1.1 Disclaimer

Every effort has been made to test the correct operation of these upgrades.

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1.2 Compatibility

The T800-20 is directly compatible with the T414B-20. Early INMOS evaluation boards were designed to use T414A-12 transputers, and thus a small modification is necessary to use T800 transputers in them. Evaluation boards with slower T414B's need memory configuration changes.

This note explains the modifications necessary to upgrade a selection of existing products.

1.3 Upgrading a B004

Your B004 may be in one of four states depending on age and state of upgrade.

B004-1 consisting T414A-12 with 1Megabyte of -15 DRAM
B004-2 consisting T414A-12 with 2Megabytes of -15 DRAM
B004-4 consisting T414B-15 with 2Megabytes of -10 DRAM
B004-4U a B004-1 or 2 which has been upgraded following D901

If you have anything different, these instructions should be sufficient to enable any upgrade.

The upgrade is divided into two sections: first configure memory for -20 transputer, then upgrade to a T800-20.

1.3.1 Memory configuration

If you have -15 memories, (eg 50256P-15), you will need to select a 6 cycle internal configuration. This is best done by replacing IC20 with the PAL `ic20 slow6`, equations listed in appendix A. Optionally, all the memories can be changed to -10, (eg HM50256P-10, MB81256-10 or equivalent), and the -10 configuration given below used.

If you have -10 memories, (eg 50256P-10), you can select a 4 cycle configuration. This is achieved using the PAL `ic20 fast4`, equations listed in appendix B.

1.3.2 Processor upgrade

The B004 is designed around a 25MHz clock. To achieve a cycle time below 66ns this must be replaced with a 5MHz oscillator and the transputers PLL enabled. To do this:

(1) If you have a T414A, replace the 10uF tantalum capacitor (directly above the transputer) with a 1uF ceramic.

(2) Replace the 25MHz oscillator with a 5MHz oscillator (available from AB European marketing, IQD etc.).

(3) Enable the transputers PLL by cutting the track linking transputer pin B1 to C2, (PCB solder side), and add a link from pin B1 to C1. The effect of this mod is to tie pin B1 to GND, previously held to VCC.

(3)

Enable the link adapter on the C003 by cutting the link from pin 11 to the large via inside the socket on the component side, and add a link from from pin 11 to pin 14. Pin 11 is now help to GND.

(5) The transputer can now be replaced with a T800-20.

1.4 Upgrading a B003

Upgrading the B003 is simple. It is merely necessary to adjust the cycle time for the memory. Provided you have -10 or -12 memories, the memory can be configured to 5 processor cycles.

If you have a B003-2 you should have a T414-20 which can be replaced directly with a T800-20.

If you have a B003-1 then the memory should be configured to 5 cycles by connecting **MemConfig** to AD6. To do this on the solder side of the board, to each of the four transputers, make the following modification;

(1) With the DIN connector to the top, in the midle of each transputers PGA are four via's. From the via pad in the top left quarter a track runs down to transputer pin J9. Cut this track.

(2) Add a link of insulated wire, connecting the via pad to pin J8, (third column from left, second row from bottom).

(3) The four transputers can now be replaced with T800-20's.

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Here is a slightly more detailed description of how to modify an IMSB004-4 so that it may take upto a 20 MHz processor.

1 Take standard IMSB004-4 and remove transputer to prevent damage.

2. Unsolder 25MHz Xtal and place a 5MHz Xtal in its place.

3. Cut track on underside of B004 from pin B1>C2 of the transputer.
   This changes the pin DisablePLL from HIGH to UNCONNECTED.
   NOTE : For a T414 this works OK as T414's have pull-down resistor on-chip, however this is not the case for the T800, therefore it is also necessary to tie B1>C1, thus holding DisablePLL LOW.
IF B1 is not tied to C1, a T800-22 will result from placing a T800 in the transputer socket. At room temperature I found this worked ok (100ns DRAMS).

4. Cut track on upperside of B004 from pin 11 on the IMSC003 to the blob on the PCB.This track is under the C003, which must therefore be removed first. The C003 has pull-downs and so pin 11 does not need grounding. This mod enables the PLL on the C003.

AT THIS STAGE IT IS POSSIBLE TO USE T414-15, T414-20, T800-20 transputers all with a 5 cycle memory interface.

5. In order to get to a 3 cycle memory interface all memory DRAMS must be swapped out. I used IMS280x-60 parts (60ns), but I am told 70's and 80's may work also.

6. Lastly it is required to modify the memory configuration so that it uses the INTERNAL configuration associated with AD4, instead of an EXTERNAL config. This is acheived by cutting the track on the upperside of the B004 between pin 19 of the F373, and pin C8 (MemConfig) of the transputer. Once this is done C8 must be connected to H8 (AD4).

7. Now plug in the transputer of your choice and the C003 and zoom away.

Regards Dave Bye INMOS/DALLAS.