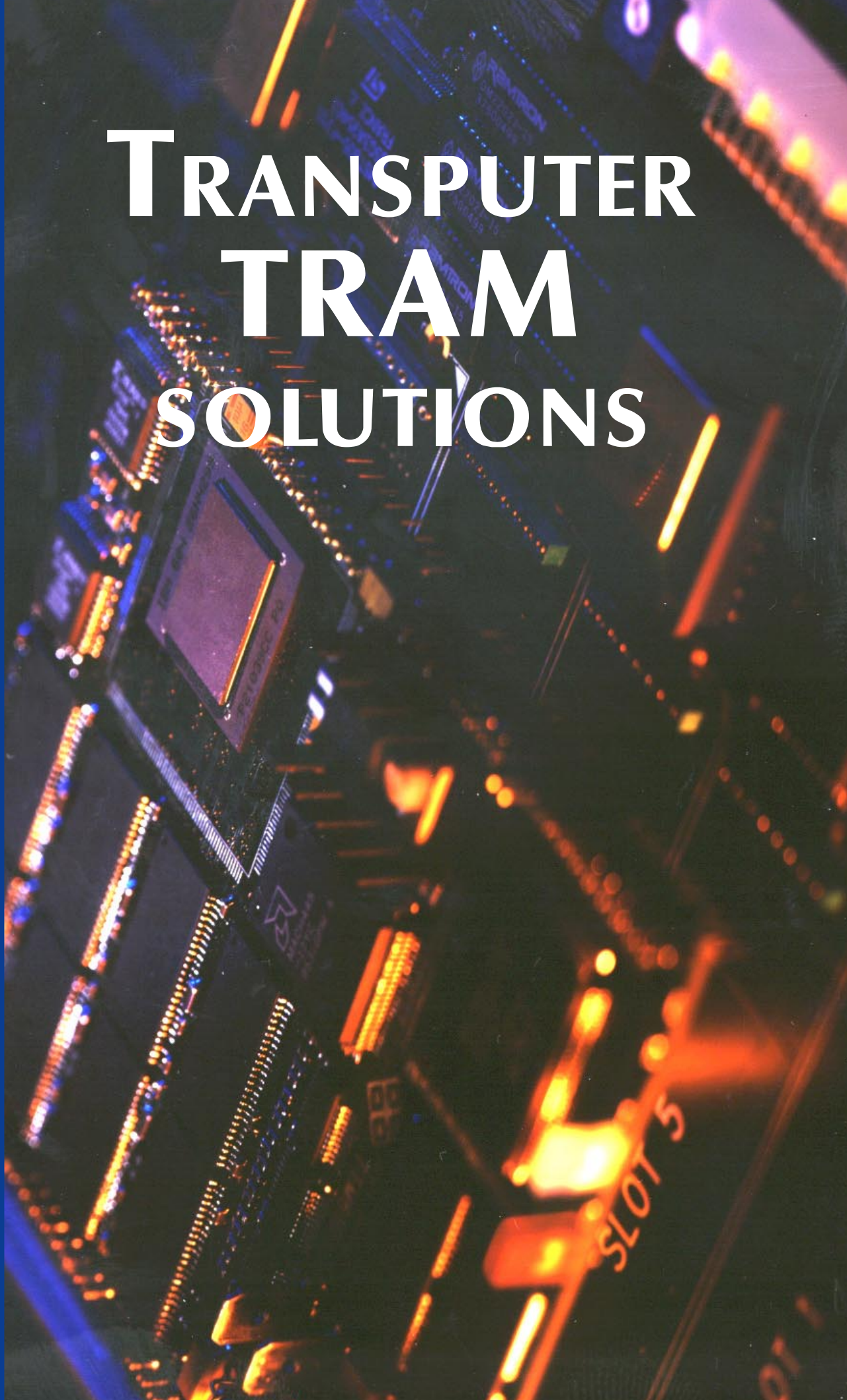
TRANSTECH

Parallel Systems

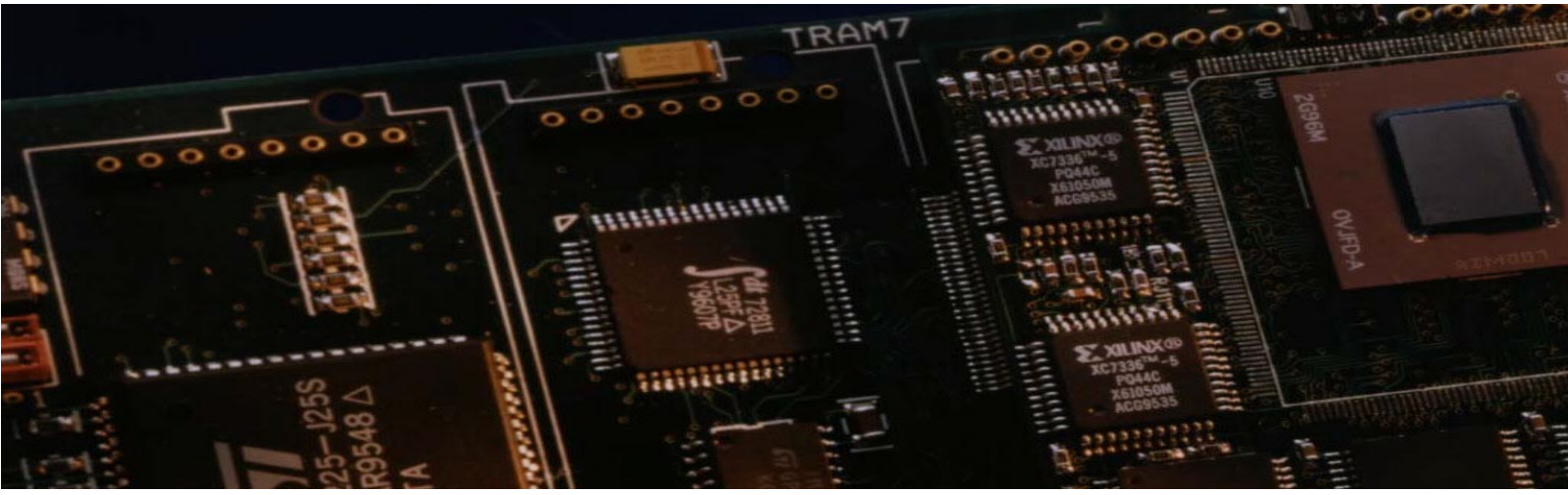
TRANSPUTER TRAM SOLUTIONS



TRANSTECH PARALLEL SYSTEMS

Transtech Parallel Systems designs and manufactures embedded multi-processing products for OEM, end-user and scientific research applications. Transtech produces signal processing and computing systems based on SGS-Thomson transputers, PowerPC processors, Analog Devices SHARC DSPs, Texas Instruments TMS320C4x and Intel i860 processors. This catalog details the Transputer products together with the PowerPC and i860 co-processors.

Transtech products are available through sales offices in New York, USA and London, England, and through a network of distributors and representatives worldwide.



Transtech Parallel Systems has been at the forefront of multi-processing systems since 1986.

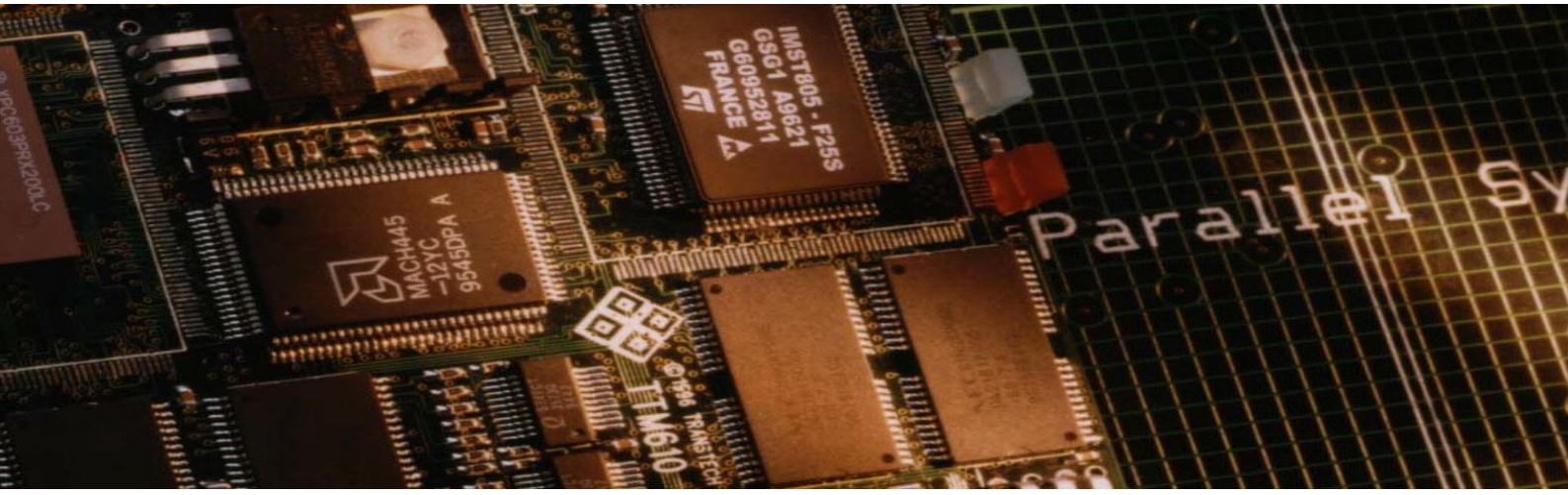
Today Transtech products are used by industrial, scientific, research and military customers to solve their high performance signal processing problems.

Over 45% of Transtech Parallel Systems staff work in research and product development. An R&D budget of 23% of sales and heavy investment in the latest design tools ensures that Transtech Parallel Systems maintain their position as the leading vendor of embedded parallel processing systems.

The use of Transtech's commercial-off-the-shelf (COTS) products brings the systems integrator the benefits of reduced time-to-market and development cost. Transtech can also supply complete turnkey systems, assembled from our standard products, to your specification.

For high-volume applications, Transtech will design custom hardware and software. This can be produced in our manufacturing facility, or you may wish to license the design rights from us.

All Transtech products are designed and manufactured for high reliability. Transtech's quality standards, for all products, are determined by the needs of major aerospace and defense customers in the USA and Europe.



All Transtech hardware products carry a comprehensive warranty, extendable by maintenance contract. Our documentation is intended to make the installation and operation of our products as straightforward as possible. In the unlikely event of any problems, our telephone support line is there to help.

Larger systems can be installed and tested on-site by our experienced customer support engineers anywhere in the world. Off-the shelf and custom enclosures are available for PC and VME-based systems.

Maintenance contracts on both hardware and software are available. A range of services from software-only through advance replacement to on-site calls are offered.

CONTENTS

SGS-THOMSON Cross Reference Guide

TRAMs

Description	SGS-THOMSON Part Number	Transtech Replacement
32Kbyte TRAM	IMSB401	TTM1
2Mbyte TRAM	IMSB404	TTM6A
1Mbyte TRAM	IMSB411	TTM3A
Differential Link TRAM	IMSB415	TTM415
64Kbyte TRAM	IMSB416	TTM22
4Mbyte TRAM	IMSB417	TTM15F
FLASH TRAM	IMSB418	TTM418
SCSI TRAM	IMSB422	TTM422
4Mbyte TRAM	IMSB426	TTM15F
8Mbyte TRAM	IMSB427	TTM18F
Ethernet TRAM	IMSB431	TTM431
16Mbyte TRAM	IMSB433	TTM19F

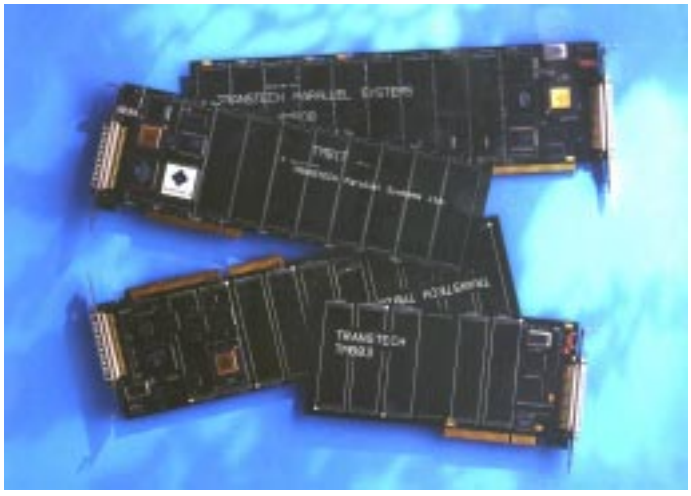
TRAM Motherboards

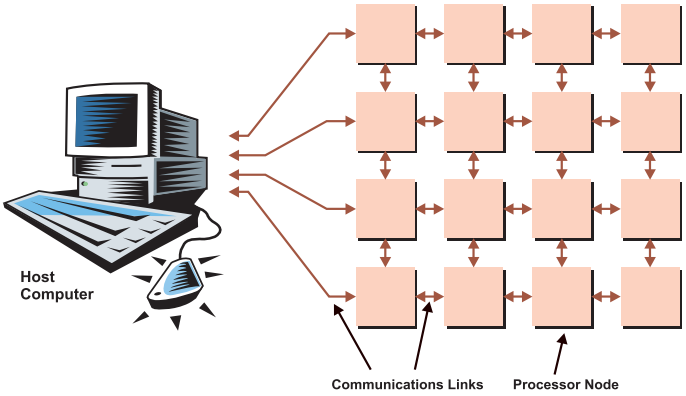
Description	SGS-THOMSON Part Number	Transtech Replacement
PC add in motherboard	IMSB008	TMB08
Double Eurocard motherboard	IMSB012	TMB12
6U VME slave motherboard	IMSB014	TMB14
6U VME master motherboard	IMSB016	TMB15

Please note: Suggested replacements may not necessarily be direct replacements and specifications may vary slightly. Please contact your nearest Transtech Sales Office for more details.

TMB03/08/16/17

PC add-in TRAM Carriers





Transtech produces 4 different PC add-in TRAM carrier boards. All of Transtech's TRAM carriers are shipped with a cable set and the Transputer Utilities software which includes a useful network test program.

TMB03: The TMB03 is a low cost interface board between a transputer and an ISA bus. The interface is compatible with the SGS Thomson IMSB008. It can accommodate up to 5 active TRAMs, though it actually has 6 TRAM slots with one being inactive to allow different size combinations of TRAMs to be fitted. It can also be used as a simple link adaptor interface between the PC and a stand alone transputer system.

The TMB08 is a full length PC add-in board with 10 TRAM slots. The interface to the PC ISA bus is identical to the TMB03. The TMB08 supports electronic re-configuration of the TRAM topology via the on-board IMSC004 link crossbar switch.

The TMB16 is similar to the TMB08 except that it has a 16-bit ISA interface. This supports higher speed data transfer between the host PC and the transputer network. For users of Transtech's i860 and Power PC products the TMB16's 16-bit interface is transparent.

The TMB17 is a PCI bus slave with an interface to a transputer network. It is a full length PC add-in card with 10 TRAM slots. It emulates the ISA interface of the TMB08 and SGS Thomson IMSB008 to enable users to migrate to the PCI without any changes to their application code. The TMB17 also includes an IMSC004 link crossbar switch.

- **Carrier boards for TRAM modules**
- **5 to 10 TRAM slots**
- **8-bit ISA, 16-bit ISA and PCI interfaces**
- **Host interface compatible with IMSB008**
- **Complete with cables and utilities**

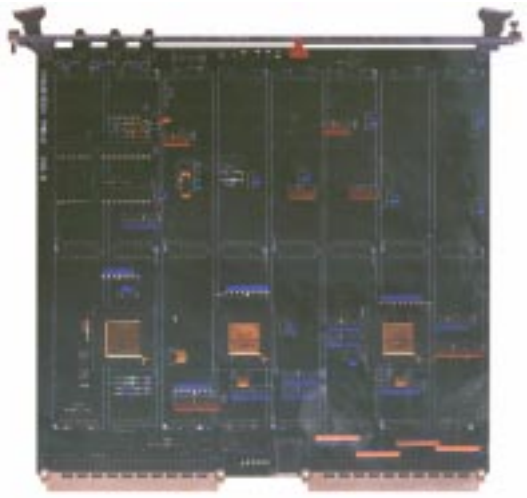
ORDERING INFORMATION

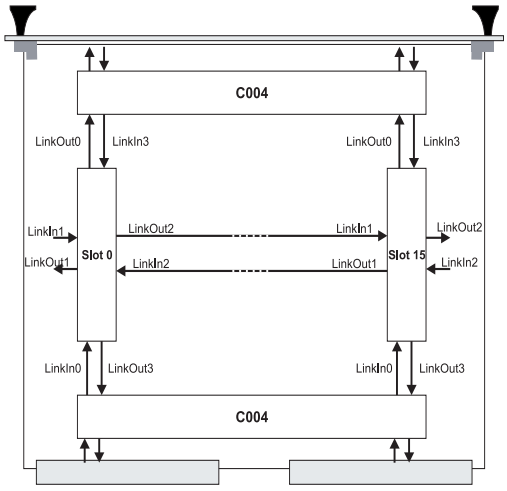
TMB03	**8-bit ISA, 5 TRAM slots**
TMB08	**8-bit ISA, 10 TRAM slots**
TMB16	**16-bit ISA, 10 TRAM slots**
TMB17	**PCI, 10 TRAM slots**

CABLE ASSEMBLIES

The boards are all supplied with a cable set which includes: 1 x 50cm reset cable, 2 x 50cm link cables, 1 x link breakout board and the appropriate number of pipe jumpers

TMB12 Double extended Eurocard TRAM Carrier





The TMB12 is a double extended Eurocard with slots for up to 16 TRAM modules. The 2 on board IMSC004 link crossbar switches allow the topology of the transputer network to be controlled from software, connecting together the links from the TRAM slots and 32 links which are taken to the edge connectors.

The TMB12 will fit into standard 6U, 220mm deep enclosures with DIN41612 connectors. Please note that the TMB12 is not compatible with VMEbus backplanes (see TMB14 and TMB15 for VMEbus interfaces).

- **Carrier board for TRAM modules**
- **16 TRAM slots**
- **Compatible with IMSB012**
- **Complete with cables and utilities**

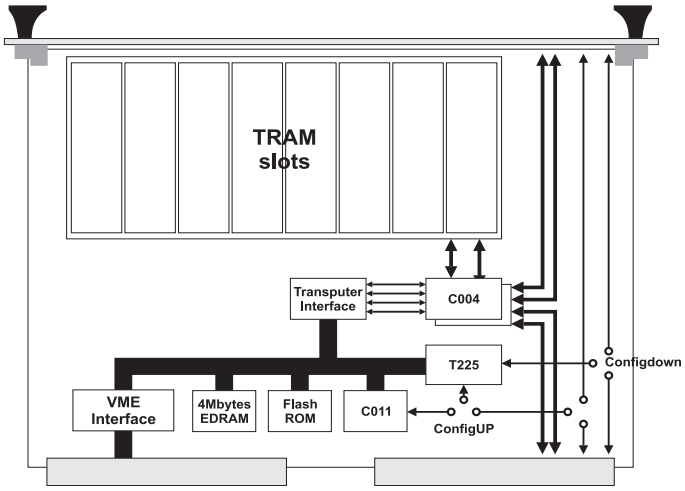
ORDERING INFORMATION

TMB12

CABLE ASSEMBLIES

The board is supplied with a comprehensive cable set

TMB14 / TMB15 TRAM Carriers with VMEbus Interface



The TMB14 and TMB15 are both 6U VME bus interface boards with 8 TRAM slots. Device drivers to interface the boards to Solaris 1.x and Solaris 2.x running on a Force 3CE SPARC based board are available.

The Transtech TMB14 is compatible with the SGS Thomson IMSB014. It has a VME bus slave interface implemented by a link adaptor mapped to the VME bus. In addition it has 2 IMSC004 link crossbar switches controlled by a 16-bit IMST225 transputer which provides re-configuration of the link topology under software control. The architecture allows any topology of transputer network to be constructed, whilst 24 transputer links are taken to the edge connectors to interface to other boards.

The TMB15 is a combined 8 slot TRAM motherboard and a high performance transputer VME slave. It has an IMST805 interface transputer with 4MBytes of fast EDRAM memory shared with the VME bus. The TRAM sites have all the links connected to a pair of socketed C004 link crossbars for electronic reconfiguration of the link topology.

The highly optimized 32-bit slave VME interface supports A24/A32 VME addressing and D32/D16/D08(EO) data transfer and flexible byte/word swapping memory regions for endian conversion. The interface transputer can boot from flash ROM or shared memory.

An IMSC011 link adaptor is interfaced to both the VME bus and the interface transputer for configuring the C004 switches (via a T225 transputer).

- **Carrier boards for TRAM modules**
- **8 TRAM slots**
- **IMSB014 compatible option - TMB14**
- **High performance DMA option -TMB15**
- **Solaris 1.x and 2.x device drivers**

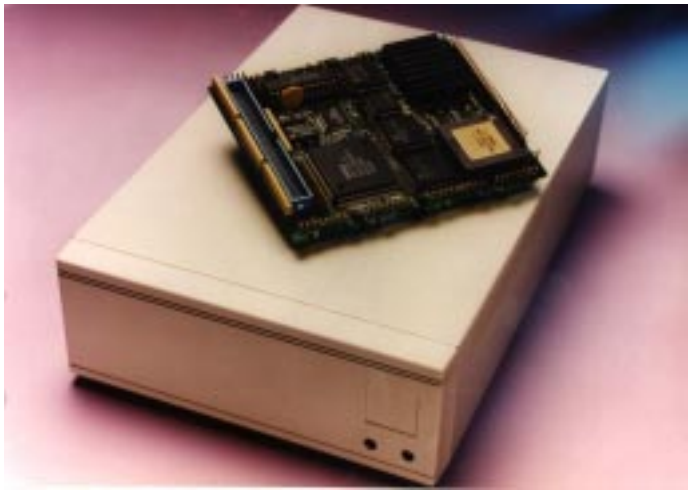
ORDERING INFORMATION

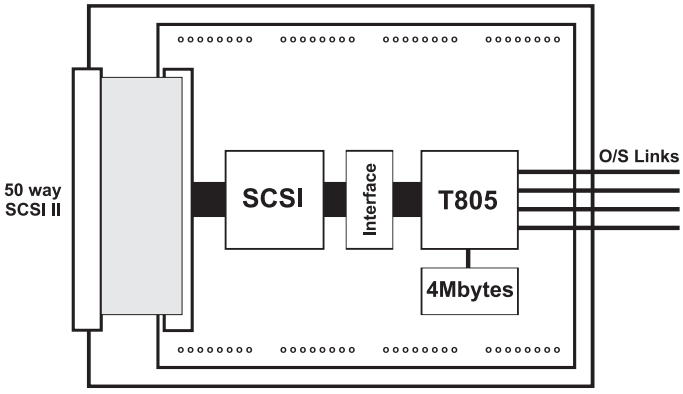
TMB14	**IMSB014 Equivalent**
TMB15	**High Performance VME slave**
TSS-TDD-Sol1	**Device Driver (Sol1 .x)**
TSS-TDD-Sol2	**Device Driver (Sol2 .x)**

CABLE ASSEMBLIES

The boards are supplied with a cable set which includes 1 x 50cm reset cable, 2 x 50cm link cables, 2 x link breakout boards and the appropriate number of pipe jumpers

Matchbox SCSI-II Host Interface for Transputer Networks





The Matchbox is a small self contained unit allowing up to 4 separate transputer systems to be connected to a UNIX workstation via a SCSI port.

Transtech supplies the Matchbox with a device driver to support the Solaris 2.x operating system running on a SPARC based host. In addition Transtech has modified the SGS Thomson iserver, aserver and network test utilities to run under Solaris 2.x.

The comprehensive manual allows developers to integrate the Matchbox with other host workstations and operating systems.

- **Multi-user transputer to host interface**
- **Plugs directly into SCSI-2 port**
- **Self contained (PSU and cooling) unit**
- **Solaris 2.x device driver**

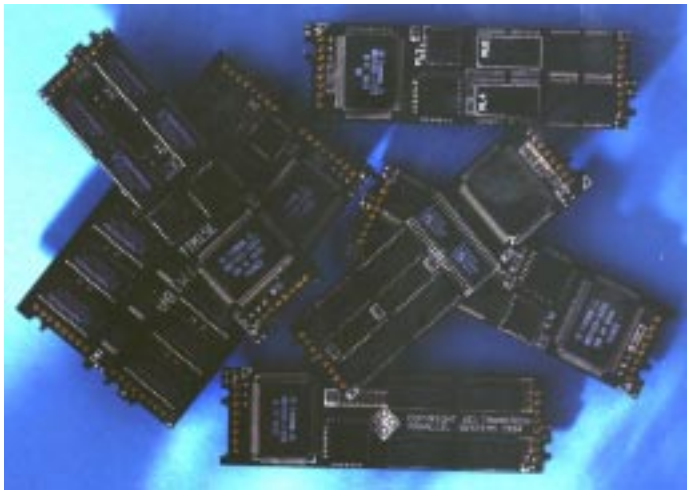
ORDERING INFORMATION

Matchbox

CABLE ASSEMBLIES
Supplied with a SCSI cable to interface to Sun SPARCstation, SCSI terminator, a link and reset breakout board and standard SGS Thomson style link and reset cables

TTM Series

Processing TRAMs



Transtech Parallel Systems' TTMxx Series are small sub-assemblies which have a transputer, some memory and optionally some application specific circuitry.

The TRAM format is defined as a standard (see opposite page) and hence it allows products from different manufacturers to be integrated together into transputer based systems.

All of Transtech's TRAMs are compatible with Transtech's range of TRAM motherboards which support varied host interfaces (ISA, PCI and VME).

Transtech's range of processing TRAMs have options for an IMST225 16-bit, IMST425 32-bit integer processors or an IMST805 32-bit floating point processor coupled to 32K, 64K, 128K, 1M, 2M, 4M, 8M or 16 Mbytes of no wait state memory.

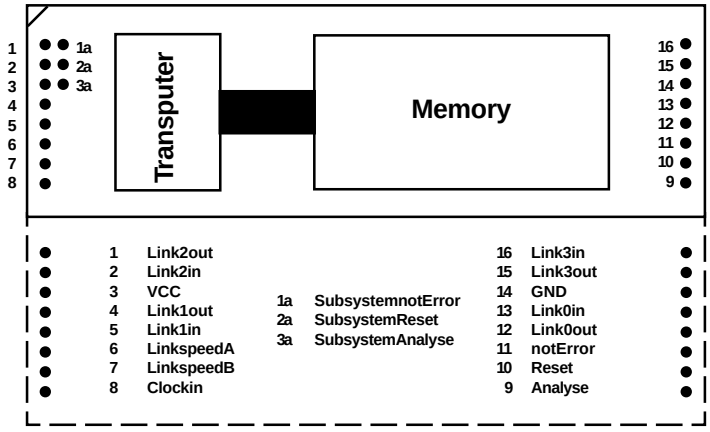
Transtech's TRAMs with 1Mbyte of RAM or more have an optional subsystem circuit which allows them to act as a master, controlling their own subsystem of TRAMs.

In addition to the processing TRAMs Transtech also produces high speed processing TRAMs (Power PC or i860) and a number of application specific TRAMs

- **T225, T425 or T805 transputer**
- **Industry standard format**
- **32K to 16 Mbyte memory options**
- **No wait state memory**
- **Subsystem circuit (on TRAMs with >1Mbyte)**
- **Small foot print: 16Mbyte TRAM takes up only 1.05”x3.66”**

The TRAM standard

The TRAM module format is an industry standard based on multiples of 26.7mm x 93mm (1.05 x 3.66 inches) - this smallest size is known as 'Size 1', a Size 2 TRAM measures 53.3mm x 93mm (2.1 x 3.66 inches) and so on. TRAM modules are compatible with Transtech's TMB series of TRAM carrier boards and are also suitable for use on carrier boards from other manufacturers who comply with the TRAM standard. Further details on the TRAM standard and TRAM Carrier Board architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.



TRAMs use 16 pins for communication with the carrier board and for obtaining power. TRAMs larger than Size 1 have more than 16 pins, the extra sets of 16 only providing extra power and ground connections . The link speed of the TRAMs is selected by two pins. When both are held low the links run at 10Mbits/second and when high at 20Mbits/second This selection is implemented by jumpers or switches on the carrier board.

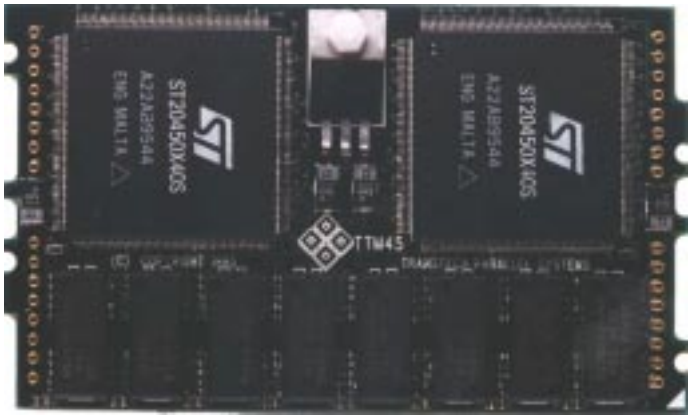
TTM Series Summary

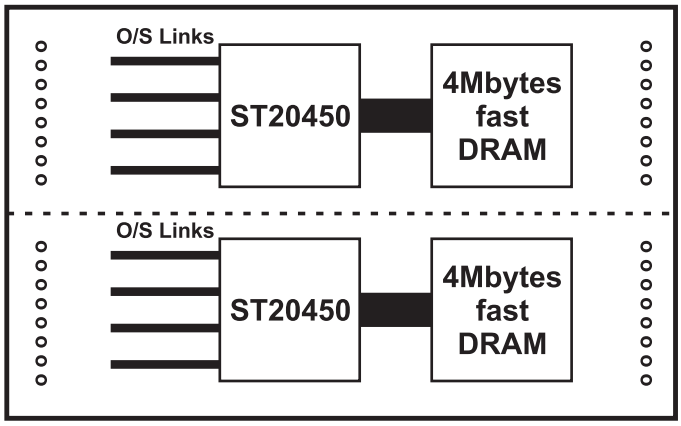
ORDERING INFORMATION

Part Number	TRAM Size	Memory (Bytes)	Processor	CPU Clock (MHz)	RAM Cycle Time (ns)	External RAM Cycles	Sub-system
TTM1-45	1	32 K	T425	25	120	3	No
TTM1-85	1	32 K	T805	25	120	3	No
TTM2A-45-F	1	128 K	T425	25	120	3	No
TTM2A-85-F	1	128 K	T805	25	120	3	No
TTM3A-45-F	1	1 M	T425	25	120	3	Yes
TTM3A-85-F	1	1 M	T805	25	120	3	Yes
TTM6A-45-F	1	2 M	T425	25	120	3	Yes
TTM6A-85-F	1	2 M	T805	25	120	3	Yes
TTM15F-45-F	1	4 M	T425	25	120	3	Yes
TTM15F-85-F	1	4 M	T805	25	120	3	Yes
TTM18F-45-F	1	8 M	T425	25	120	3	Yes
TTM18F-85-F	1	8 M	T805	25	120	3	Yes
TTM19F-45-F	1	16 M	T425	25	120	3	Yes
TTM19F-85-F	1	16 M	T805	25	120	3	Yes
TTM22	1	64K	T225	25	80	2	No

TTM45

ST20450 Processing TRAM





The TTM45 is a size 2 TRAM with two ST20450 processors each with 4Mbytes of fast page mode DRAM. Electrically the TTM45 is two independent size 1 TRAMs, i.e. there are no link connections on the module between the two processors.

The ST20450 is a high performance 32-bit micro-controller based on the ST20C4 macrocell core. It provides 16Kbytes of on-chip memory for fast access to local code, a vectored interrupt controller, four OS-Links and a multi-bank external memory controller.

The CPU contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the 16Kbyte on-chip memory, which can store data or program code. The on-chip SRAM provides 160Mbytes/s internal data bandwidth, supporting pipelined 2-cycle internal memory accesses at 25ns cycle times. Sustained transfer rates into external page mode DRAM are up to 80Mbytes/s.

The ST20450 has an OS-Link based serial communications subsystem. OS-Links use an asynchronous bit-serial (byte stream) protocol, each received bit is sampled five times, hence the term *over-sampled links* (OS-Links). Each OS-Link provides a pair of channels, one in and one out. The four full duplex OS-Links on the ST20450 are driven by individual DMA engines independent of the CPU. The links have programmable unidirectional data rates of 10 or 20 Mbits/s, giving a bidirectional bandwidth approaching 3Mbytes/sec.

- **Industry standard size 2 TRAM format**
- **Dual ST20450 Processors**
- **High performance, up to 80 MIPs**
- **Compatible with T2, T4 and T8 TRAMs**

TECHNICAL DATA

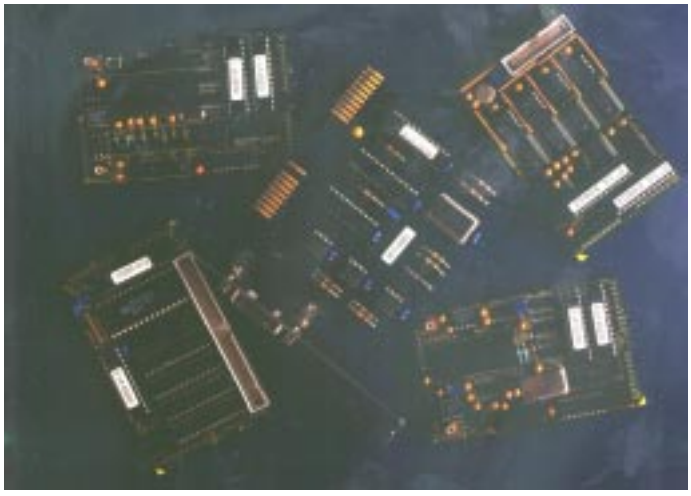
Number of OS-Links:	8 (4 per processor)	
Subsystem Logic:	No	
Memory Speed:	60ns	
Dimensions:		
TRAM Size:	2	
Length:	93mm	
Width:	53.1mm	
Height:	4.5mm	*(Above top face of PCB)*
Mass:	60g	
Operating Temp:	0-50 °C	
Power Supply:		
Voltage:	4.75 - 5.25V	
Dissipation:	TBA	*(maximum)*

ORDERING INFORMATION

TTM45-1-40	**TTM45 with single ST20450 CPU**
TTM45-2-40	**TTM45 with two ST20450 CPUs**

Please note: The SGS Thomson 4th generation toolsets are required to use the TTM45 as this supports ST20450 code

Analog I/O TRAMs



The range of Analog and Digital I/O TRAMs available are all compatible with Transtech's TRAM motherboards. Included in the range are 5 analog input modules, 2 digital to analog converter modules and 4 digital I/O modules.

Analog to Digital Converters

The ADT108x range are 12-bit A to D modules operating at up to 100ksamples/sec.
ADT108A: 8 channel with differential inputs.
ADT108B: 16 channels with single ended inputs.
ADT108C:16 channels with differential inputs.
ADT108D: 32 channels with single ended inputs.

ADT112: 2 channel, 16-bit A to D converter that can operate up to 200 Ksamples/sec and has a 1024 word FIFO buffer.

Digital to Analog Converters

DAT202: 2 channel, 16-bit, 200 Ksample D to A module.

DAT208: 8 channel, 12-bit, 50 Ksamples/sec D to A module.

Digital Input/Output Modules

IOT332: 32 channel TTL level I/O module.

IOT336: 32 channel TTL level I/O module with an on-board transputer (option of either T400, T425 or T805).

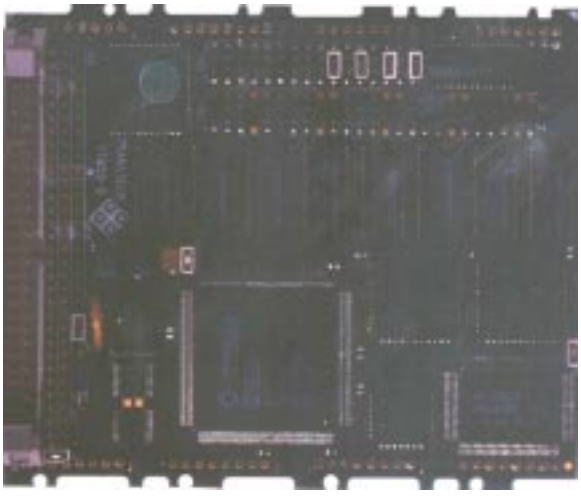
- **Analog to Digital**
  - **Up to 200K samples/sec**
  - **2 - 32 channels**
  - **12 & 16-bit options**
- **Digital to Analog**
  - **Up to 8 channels**
  - **12 & 16-bit options**
- **Digital I/O TRAM modules**
  - **32 channels**
  - **Option for transputer on-board**

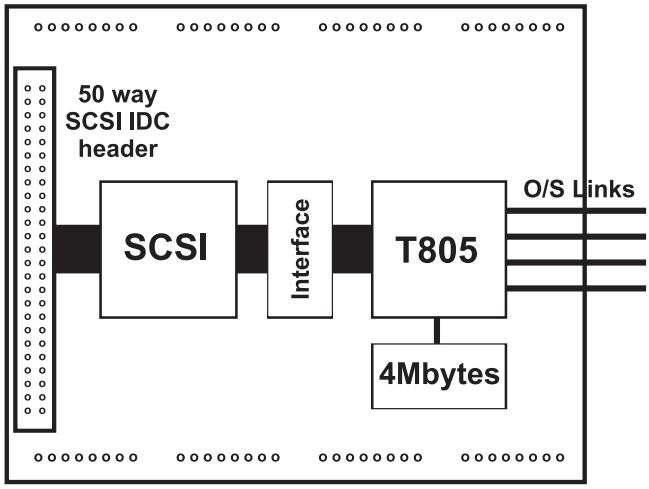
ORDERING INFORMATION

ADT108A	**8 ch DI, 12-bit, 100KHz A/D**
ADT108B	**16 ch SE, 12-bit, 100KHz A/D**
ADT108C	**16 ch DI, 12-bit, 100KHz A/D**
ADT108D	**32 ch SE, 12-bit, 100KHz A/D**
ADT112	**2 ch DI, 16-bit, 200KHz A/D**
DAT202	**2 ch, 16-bit, 200KHz D/A**
DAT208	**8 ch, 12-bit, 50KHz D/A**
IOT332	**32 ch TTL I/O**
IOT336-4-A	**32 ch TTL I/O with T400**
IOT336-4-B	**32 ch TTL I/O with T425**
IOT336-4-C	**32 ch TTL I/O with T805**

TTM50

SCSI TRAM





The Transtech TTM50 is a TRAM that provides a transputer to SCSI-2 interface. It is suitable for connecting a wide range of SCSI devices, including disks, tapes, CD-ROM and workstations to transputer networks.

The TTM50 can be supplied to support both single ended or differential SCSI (factory build option), and can also if required be supplied with device drivers to interface it to a Sun SPARCstation running Solaris 2.x (to be used in the same manner as the Transtech Matchbox, see page 9).

The TTM50 is supplied with extensive software support which includes:-

Low level libraries to program at the SCSI command level, both as an initiator and as a target are supplied. SCSI disconnects are fully supported in both modes. The library is multi-threaded and can support transactions with many logical units on the SCSI bus.

The Transtech File System (TFS) provides a UNIX like hierarchy of files and directories, with ownership and protection modes, hard links to files and multi-threaded access.

Client-server operation of the file system allows processes anywhere in the transputer network to access the file system using the standard I/O mechanisms.

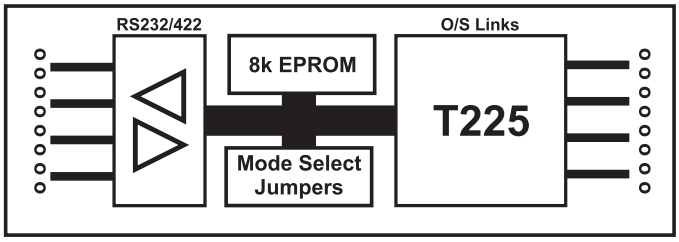
The TFS shell provides convenient administration of the file system including backup and restore of entire directory structures from ANSI standard tar files.

- **SCSI-2 to transputer interface**
- **Initiator and target mode support**
- **Low level SCSI library**
- **TFS file system**
- **Standard size 4 TRAM format**

ORDERING INFORMATION

TTM50S	**Single ended version**
TTM50D	**Differential version**

TTM21 / TTM23 RS232 / RS422 to transputer interface



The Transtech TTM21 and TTM23 respectively enable up to four RS232 or RS422 connections per TRAM to be made to a transputer network. The RS232 and RS422 interfaces support serial transfer rates of 9.6Kbaud and can buffer up to 256 bytes internally. This is more than adequate for interfacing a mouse, keyboard, printer or instrumentation.

The TTM21 and TTM23 TRAMs are logically identical, except they support different serial I/O standards. By default, the TTM21/TTM23 TRAM can be treated as a standalone transputer link to RS232/RS422 interface. Alternatively the serial interface can be configured in software. In this mode multiple TTM21 and or TTM23 TRAMs can be daisy-chained allowing large numbers of RS232 and or RS422 connections to be controlled from a single transputer link. Transfer rates in software mode can be up to 9.6Kbaud on up to four ports and up to 38.4Kbaud on one.

Transputer libraries, include files and example programs are supplied for Inmos ANSI C and occam to aid development of applications using the TTM21/TTM23 in software mode.

Both the TTM21 and the TTM23 TRAM have an SGS Thomson T225 transputer fitted which is normally used in boot from ROM mode. The 8K EPROM contains the code executed by the T225 transputer after reset.

The TTM21 TRAM can support three types of RS232 interfaces which are characterized by the number of cable wires used. These are three, five and seven wire modes. The equivalent RS422 modes supported by the TTM23 TRAM are four, eight and twelve wire modes.

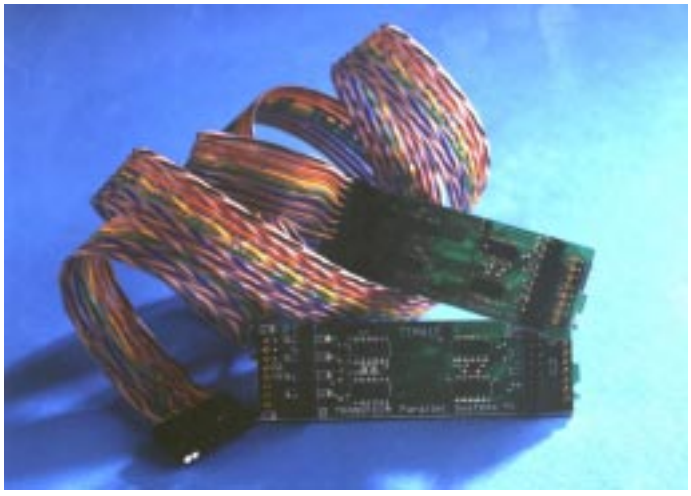
- **RS232 or RS422 interface**
- **Up to 4 serial interfaces per TRAM**
- **Up to 38.4 Kbaud**
- **Standard size 1 TRAM format**

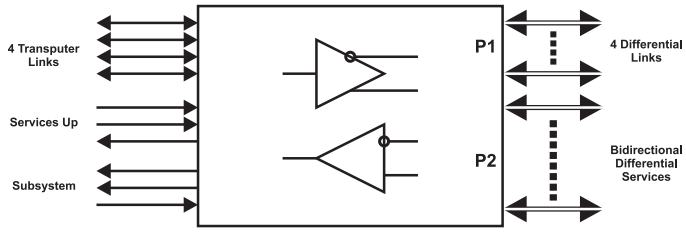
ORDERING INFORMATION

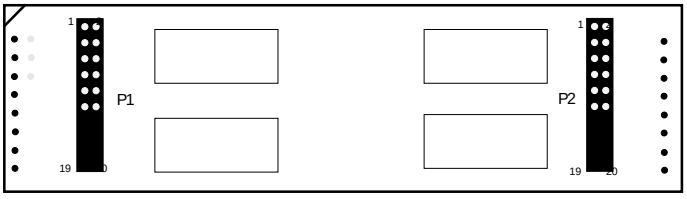
TTM21 RS232 interface TRAM
TTM23 RS422 interface TRAM

TTM415

Differential Link TRAM







The TTM415 Differential Interface Buffer TRAM allows connections between transputer systems which are not in the same electrical environment. No common ground between the two systems is required, reducing earthing problems. Cable lengths up to 10m can be operated at the full 20Mbits/s link speed. Longer cables up to 100m can be used at lower link speeds.

The TTM415 contains only differential drivers & receivers and associated signal conditioning components. This allows correct link behavior to be maintained with no software changes needed. Alternative buffering techniques that decode the link packets and forward them using a different coding technique require software modifications because more than one byte may be in transit at any one time.

Two 20-pin connectors, labelled P1 and P2, carry the RS422 differential signals from the top face of the TRAM. These are standard 0.025inch square post gold pin headers with two rows of ten pins on 0.1inch centers. P1 carries the link signals, P2 carries the system control signals.

The TTM415 is designed for use with twisted-pair cables with a characteristic impedance of 100W. Cables longer than 10m may not to operate reliably at 20Mbits/second. Transtech recommends that unshielded twisted pair cable be used. To comply with FCC and EU EMC regulations, these cables should only be used within a shielded enclosure.

For normal operation between two TTM415s the following cable wiring details should be followed. The recommended cable type is Amphenol Spectrastrip, part #1352802-316.

- **Direct replacement for IMSB415-0 and IMSB415-1**
- **20Mbit/sec link operation**
- **Size 1 TRAM**

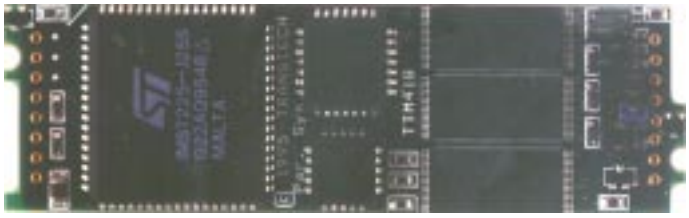
P1		P2	
Pin	*Signal Name*	*Pin*	*Signal Name*
1	Link0Out-	1	DownReset-
2	Link0Out+	2	DownReset+
3	Link0In-	3	DownError-
4	Link0In+	4	DownError+
5	Link1Out-	5	DownAnalyse-
6	Link1Out+	6	DownAnalyse+
7	Link1In-	7	UpReset-
8	Link1In+	8	UpReset+
9	Link2Out-	9	UpError-
10	Link2Out+	10	UpError+
11	Link2In-	11	UpAnalyse-
12	Link2In+	12	UpAnalyse+
13	Link3Out-	13	NC
14	Link3Out+	14	NC
15	Link3In-	15	NC
16	Link3In+	16	NC
17	Cut Short	17	NC
18	NC	18	NC
19	Cut Short	19	Cut Short
20	NC	20	Cut Short

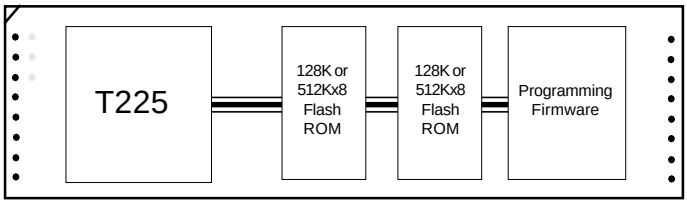
ORDERING INFORMATION

TTM415-0	**Single TTM415 TRAM**
TTM415-1	**Pair of TTM415 TRAMs plus 1 meter cables**

TTM418

FLASH ROM TRAM





The TTM418 Flash ROM TRAM is designed primarily for configuring and bootstrapping transputer networks in embedded systems.

After reset, the TTM418 feeds a program stored in the ROM through one of its four OS-Links. On-board software allows the Flash ROM to be reprogrammed without removing the ROM devices from the board or the TTM418 from an assembled system. Programming is via a simple protocol on one of the OS-Links. Safeguards are provided against accidental erasure or reprogramming. The Flash ROM devices can be reprogrammed in excess of 10,000 times.

In a system incorporating a TTM418, reset signals from the TRAM (subsystem services) are used to reset the target system. The TTM418 incorporates power-on reset circuitry and so can provide power-on reset and automatic start-up for the target system. The TTM418 can have one or two link connections to the target system. One link carries program code to the target, the other can be used to configure C004 Link Switches prior to bootstrapping the target.

During software development the TTM418 can be installed into the system as it would be in the finished product. The development host is connected to the TTM418 using the *transparent mode*.

Resident software in a separate memory on the TTM418 allows for device programming, system booting and the various debug and transparency modes. The firmware is used by sending commands to the TTM418 in *bootstrap mode* on any link. When a command is received on a link, an appropriate action is made, with a response on the same link.

- **Direct Replacement for SGS Thomson IMSB418**
- **Non-Volatile RAM (256Kbyte or 1Mbyte)**
- **In-System Reprogrammable**
- **On-Board Programming Firmware**
- **16-bit IMST225 transputer**
- **Standard size 1 TRAM format**

ORDERING INFORMATION

TTM418-256	**256kbyte option**
TTM418-1024	**1Mbyte option**

Custom Design Service

In addition to standard products, Transtech can also provide custom solutions. These may be appropriate where the standard boards need modifications for slightly different functionality, or where volumes dictate that the boards need re-designing to reduce cost.

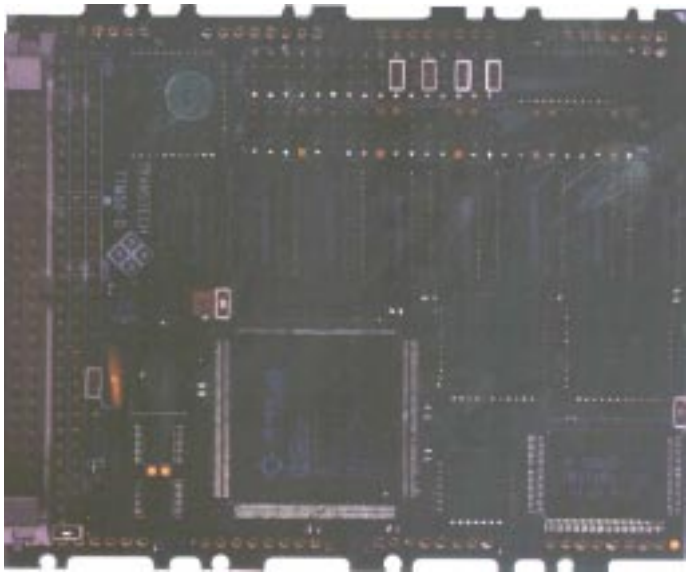
Transtech's team of development engineers have unrivalled transputer design experience and can quickly provide custom solutions to meet the needs of the customer.

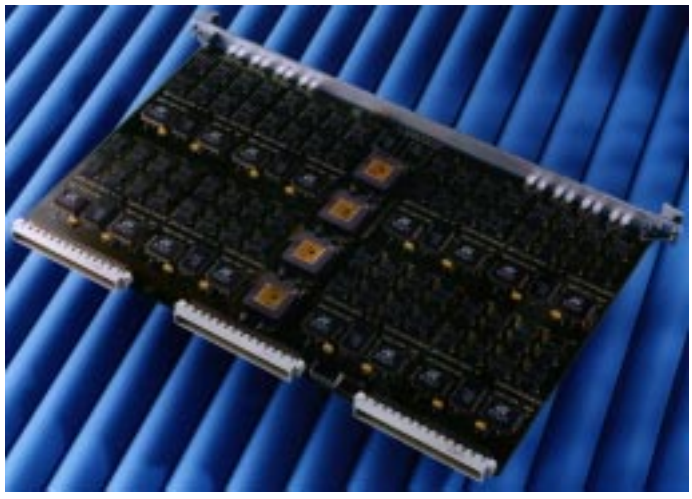
- **Custom board design**
- **Extra functionality**
- **Reduced cost on large volumes**
- **Based on standard designs**
- **Reduced time to market**

The board below is a Transtech SCSI TRAM. The standard product is used to interface SCSI disks to transputer networks.

This product has been custom modified in different ways for several customers

- to connect to differential SCSI disks for a major Japanese electronics corporation
- to provide the interface to a host workstation for a manufacturer of financial dealing desks
- to interface a VME bus master to a custom transputer board within an operational military sonar system





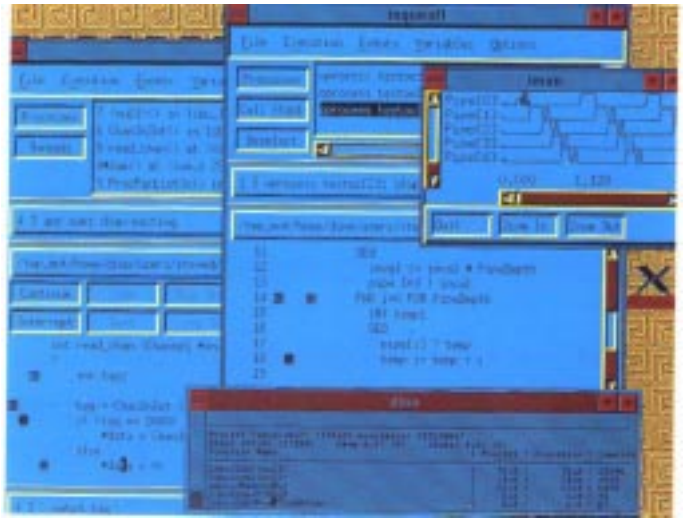
The board pictured above is a 9U x 220mm board with 16 transputers and up to 16 Mbytes of fast page mode DRAM per board.

ORDERING INFORMATION

For further details contact your nearest Transtech sales office

SGS-Thomson Toolsets

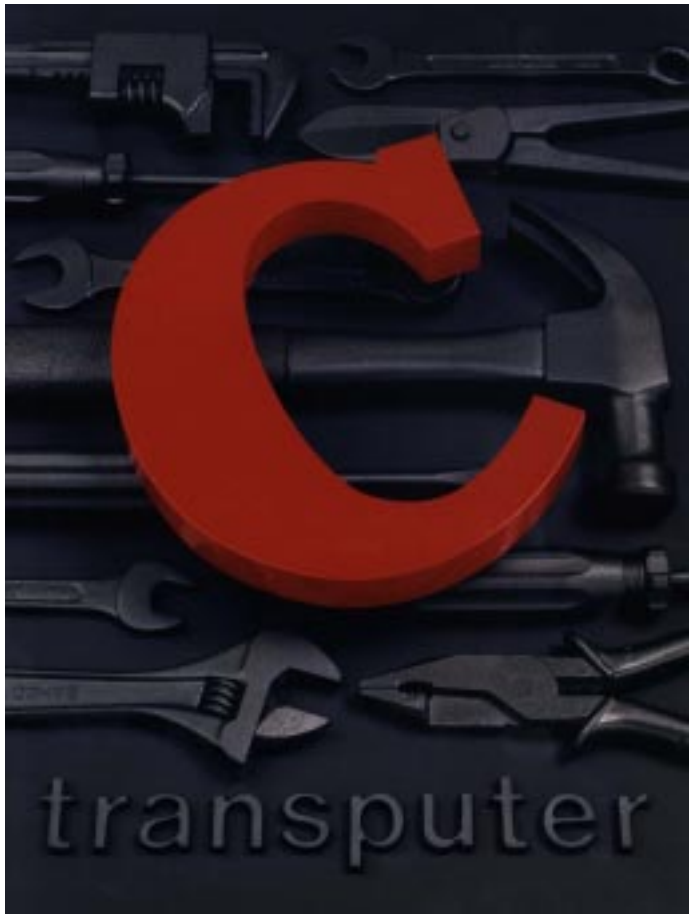
Development Software



The SGS Thomson Toolsets offer professional development environments for targeting transputer applications. The toolsets incorporate a complete set of tools and libraries for developing transputer applications ranging from a low-cost single processor system to highly parallel multi-processor embedded systems.

The SGS Thomson toolsets allow code development for the transputer in C or occam hosted by either a PC or Sun development workstation. The code building tools run on the host machine while the target hardware is programmed and debugged via the standard transputer links. This interface is also used for provision of host operating system services for transputer applications.

Included in the latest toolsets is the SGS Thomson INQUEST advanced debugging environment which provides users with an extremely flexible, high performance and high functionality debugger for developing applications running on one or more transputers.



- **Targets all T2, T4 and T8 transputers**
- **PC and Sun hosted systems**
- **ANSI C and Occam compilers**
- **Assembly language programming**
- **Automated message routing**
- **INQUEST debugger included**

ORDERING INFORMATION

IMSD4405	**Occam Toolset, Sun hosted**
IMSD4414	**ANSI C Toolset, Sun hosted**
IMSD7405	**Occam Toolset, PC hosted**
IMSD7414	**ANSI C Toolset, PC hosted**

PowerPC - Processor Overview

Backed by many of the world's largest computer companies and a wide variety of software vendors, PowerPC has become *the* processor of choice for a new generation of high performance, real-time systems.

Transtech's current PowerPC products are based upon the PowerPC 603eV and 604eV processors.

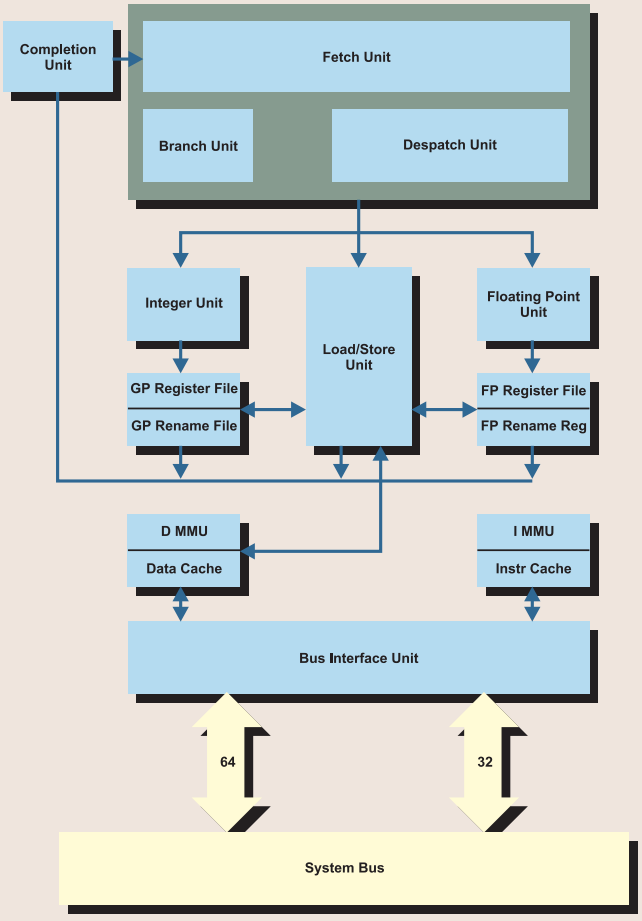
TTM610

PowerPC 603eV

The PowerPC 603eV is a superscalar RISC microprocessor capable of issuing three instructions per clock cycle into five independent execution units.

The ability to execute multiple instructions in parallel, to pipeline instructions and the use of simple instructions with rapid execution times gives the PowerPC 603eV its high performance.

The PowerPC 603eV's dynamic power management system selectively activates functional units as they are required by the executing program. Unused functional units power-down automatically without affecting performance, software execution, or external hardware.

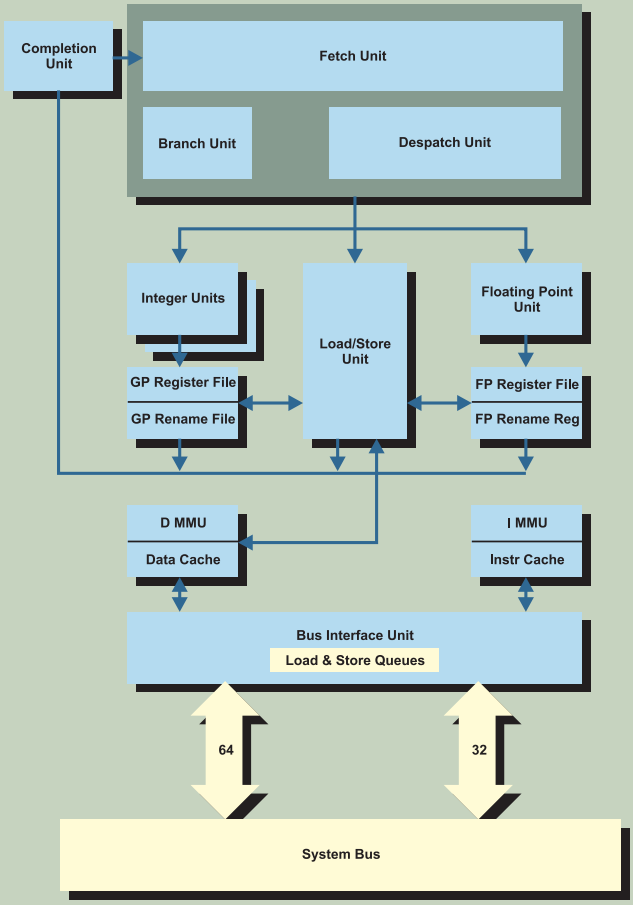


603eV has 5 independent execution units

- integer unit
- floating point unit
- branch processing unit
- load / store unit
- system register unit

604eV has 7 independent execution units

- two, single cycle integer units
- multi-cycle integer unit
- floating point unit
- branch processing unit
- load / store unit
- condition register unit



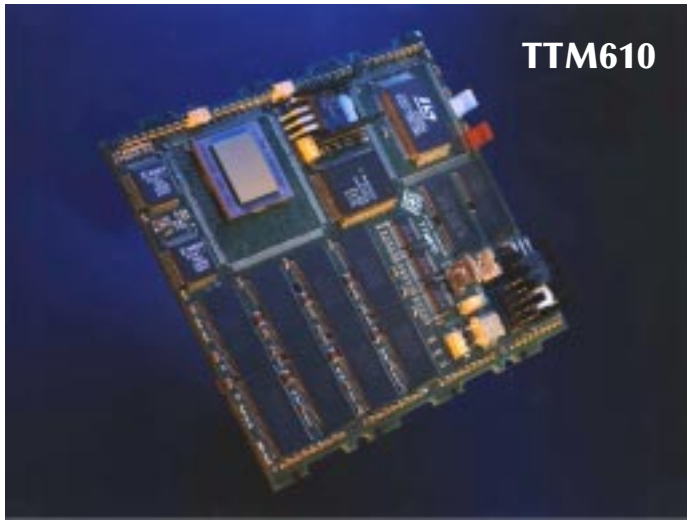
PowerPC 604eV

The PowerPC 604eV is a superscalar RISC microprocessor capable of issuing four instructions per clock cycle into seven independent execution units.

The PowerPC 604eV uses dynamic branch prediction to improve the accuracy of instruction prefetching. Dynamic branch prediction, combined with the ability to speculatively execute through two unresolved branches, minimizes pipeline stalls and allows the multiple execution units to provide a high level of efficiency and throughput. While the PowerPC 604eV supports out-of-order execution, in-order instruction completion assures precise exceptions.

The PowerPC 604eV has separate, physically addressed, 4-way associative, 32KByte instruction and data caches.

PowerPC TRAMs



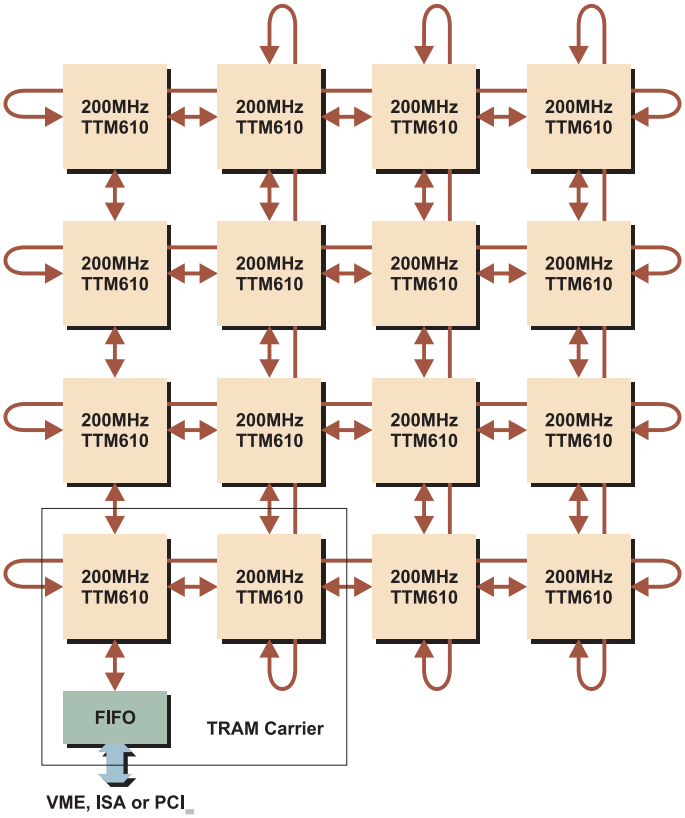
Many of Transtech's existing customers have been tied by their software to the SGS Thomson transputer. Transtech can now offer easy to integrate PowerPC nodes for transputer systems. Using VTK (virtual transputer kernel) it is possible to port software written for the transputer C Toolset quickly to the PowerPC with no source code changes. The TTM610 is a size 4 PowerPC TRAM module for scalable, high performance multi-processor solutions.

Power PC

The TTM610 uses the fastest PowerPC 603eV and 604eV processors for maximum performance. The high clock speed together with large on-chip caches (32K/603eV and 64K/604eV) yields practical compute power. Floating point performance for a 200MHz PowerPC 603eV is in excess of 40MFLOPs sustained (133MFLOPs peak).

High Speed Memory

16 or 32Mbytes of high speed Synchronous DRAM (SDRAM) is supplied giving the PowerPC a performance advantage. Shared between the PowerPC and T805, the SDRAM is the mechanism by which they communicate.



Communications Processor

In parallel with the PowerPC is a T805 to handle the TTM610 I/O by maintaining 4 simultaneous 20Mbit/sec links. These links provide connection to other TTM610 modules (or other TRAMs) to provide scalable parallel processing systems.

In system operation, the PowerPC has no direct communication beyond its memory. Instead, the PowerPC cooperates with the T805 through shared memory with high level command and data packets. In this way the T805 becomes a 'proxy' processor forwarding and receiving data on behalf of the PowerPC, which allied to the programming model makes the PowerPC on the TTM610 appear to the programmer as if it were a "super" transputer.

Scalable Multi-Processing

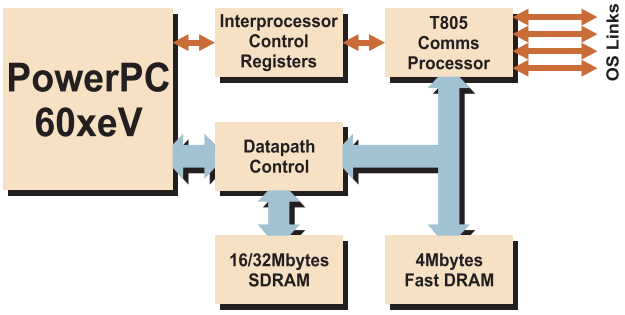
Designed to be used in clusters, the TTM610 can be used to construct various network topologies from simple processor pipelines to complex meshes with 100s of PowerPC nodes per system. Within an array each processor can communicate with other TRAMs via one or more of the four 20Mbit/sec bidirectional links. Since each of these links allows communication directly with other TRAM modules over a twisted wire pair, both hardware and software is independent of its host carrier board.

Carrier Boards

To mount the TTM610 Transtech offers a range of TRAM carrier boards for VME, PCI, ISA and other environments. When fitted to the carrier boards the TTM610s communicate to each other directly, bypassing the host. For host to TRAM communication, one of the 20Mbit/sec links can be routed to the host interface. This provides a *front end* for system I/O and a means to boot application code.

TTM610

Power PC TRAM



TTM610
Block Diagram

The TTM610 is constructed as a size 4 TRAM module with a 200MHz PowerPC, up to 32Mbytes of main memory and a T805 communications processor which has 4Mbytes of private local memory. The two processors exchange data in shared memory, with interrupts and full bus locking to synchronize such transactions.

The advanced design of the memory interface on the TTM610 gives 278 Mbytes/sec memory to memory copy when using a 603eV running at 200 MHz.

The TTM610 can be used just like transputer TRAMs. They are mounted on standard TRAM motherboards, and using the Transtech PowerPC development tools are integrated into transputer networks. The users in effect declares the Power PC TRAM as a "super" transputer. The 4 transmit/ receive communications links can be run simultaneously each achieving 20 Mbits/sec

The TTM610 is available with a PowerPC 603eV or 604eV running at 200 MHz with a 66 MHz bus speed, and either 16 or 32 Mbytes of Synchronous DRAM.

Using the PowerPC in TRAM format, the TTM610 allows the integration of other transputer based TRAM modules with the PowerPC.

- **200MHz PowerPC 603eV or 604eV**
- **Industry standard format (size 4 TRAM)**
- **16 or 32 Mbyte memory options**
- **66 MHz processor bus**
- **T805 Communication Processor**

TECHNICAL DATA

Card Format:	Size 4 TRAM
Physical Dimensions:	4.35" x 3.66" (110 x 93mm)
Power Requirements:	3A @ 5V 603eV @ 200 MHz (32 Mbytes) 8A @ 5V 604eV @ 200 MHz (32 Mbytes)

ORDERING INFORMATION

TTM610-E-16	**PowerPC TRAM with 603eV @ 200 MHz and 16 MByte RAM**
TTM610-E-32	**PowerPC TRAM with 603eV @ 200 MHz and 32 MByte RAM**
TTM610-F-16	**PowerPC TRAM with 604eV @ 200 MHz and 16 MByte RAM**
TTM610-F-32	**PowerPC TRAM with 604eV @ 200 MHz and 32 MByte RAM**

PowerPC Development Tools

Specially developed for the Transtech Power PC family is a set of tools for multi-processor applications which specifically address the needs of parallel processing. These tools include: TTOOLs - kernel, programming model, host services; C/C++ compilers and debuggers. Expertise in developing software environments for multi-processing, allows Transtech to offer a single programming model to customers which can be used to port code to the PowerPC TRAMs from transputers and is also compatible with Transtech's other PowerPC VME products.

TTOOLs Host Components

- I/O Communications Libraries
- Profiler
- Configurer
- Loader
- Server I/O daemon

TTOOLs Target Components

- VTK - Kernel
- I/O Communications Libraries
- Real-Time Extensions
- Host I/O Libraries

Split into two parts, TTOOLs provides both a run-time target environment and a set of host based utilities. The target portion includes a real-time kernel, an I/O communications library, and a host server library which allows applications to use remote system resources.

The kernel "VTK" (Virtual Transputer Kernel), a key component of TTOOLs, is a modern compact micro-kernel to provide fast and efficient multi-tasking with the added benefit of channel based communications. Layered on VTK is the I/O communications library.

The I/O communications library is an extension of the SGS Thomson transputer interface library, this ensures that code written for the SGS Thomson C toolset can be recompiled, reconfigured and run - a low risk migration path from Transputer to PowerPC.

TTOOLs and PowerPC provides extra benefits, ideal for real-time applications over tranpsuter based systems. These enhancements available through an extensions library which includes preemptive scheduling and 256 priority levels.

The third library provided by TTOOLs allows application programs to use system resources provided by a host computer. These services include serial I/O, access to system information (environment variables, etc.) and file I/O.

Host based components of TTOOLs are profiling tools to analyze optimal task distribution across processor nodes, a configurer which produces network boot files, the libraries used when compiling the applications, a loader to download the tasks and an application program which acts as the server agent for the tasks running on the PowerPC targets.

VTK

Features	Benefits
Can reuse existing Transputer C code	Faster program development Reduced cost Reduced risk Upgrade to PowerPC technology for higher performance
Channel based communications	Simplifies inter-task communications using Transputer model
Fast Switching between processes	Efficient, responsive and high performance operation
Multi-threaded	Multiple tasks can run on each processor
Tasks can be placed on any processor	System performance can be optimized
Timers	Real-time control and scheduling
256 priority levels	Ensures critical tasks get CPU time
Semaphores	Simplifies resource allocation and inter-task synchronization
I/O server services	Processes have access to advanced I/O facilities
Round-Robin or preemptive scheduling	Choice of fair or priority modes to suit application

Development Systems

Transtech can provide a number of different development systems for PowerPC products which require either a PC running Windows95/NT or a Sun SPARCstation running SunOS4 or Solaris 2.x.

Development System Choices

- WIndows95/NT, SunOS4 or Solaris 2.x
- PC or Sun Hosted
- PC add-in or VME target systems

TTOOLS Development for TTM610

The TTM610 requires a transputer link connected to the host which is provided by the appropriate TRAM carrier card, on to which the TTM610 is mounted. The carrier card can be an ISA or PCI format in a PC or alternatively it can be 6U VME card housed in a VME enclosure. The simplest system in a PC only requires a TTM610, TRAM carrier card and TTOOLS development software with a C compiler.

TTM610 development in a VME enclosure requires a SPARC based VME master. The host tools can run on this VME board, or on a separate machine connected via ethernet. Program loading and debugging use the VME backplane to access the PowerPC processors. Transtech can supply complete, fully configured and tested VME development systems.

ORDERING INFORMATION

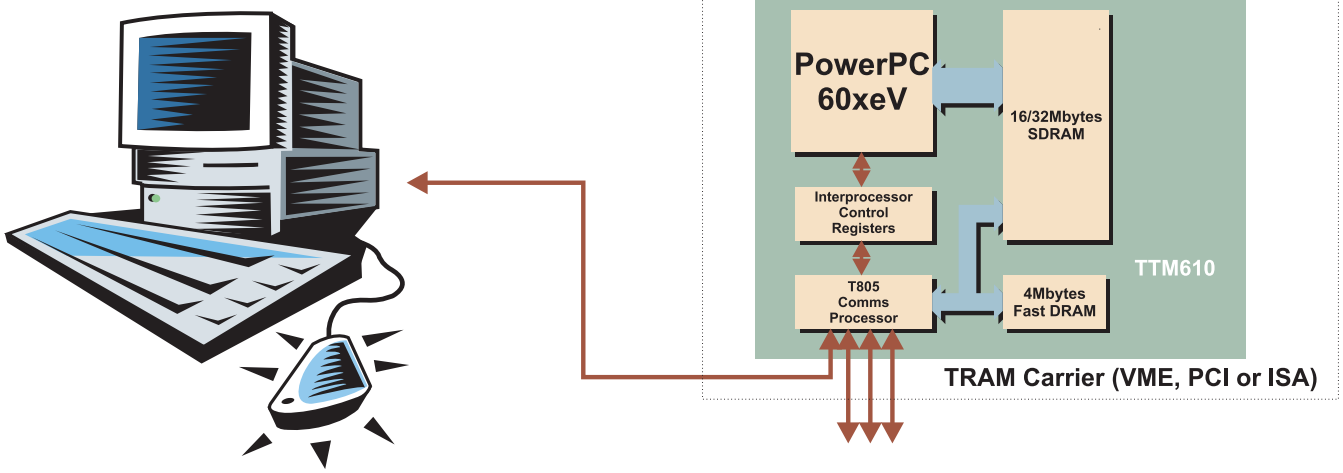
Development Software Tools

TSSPPC-T-S1	TTools - Solaris 1.x
TSSPPC-T-S2	TTools - Solaris 2.x
TSSPPC-T-PC	TTools - Windows/DOS
TSSPPC-C-S1	C Compiler - Solaris 1.x
TSSPPC-C-S2	C Compiler - Solaris 2.x
TSSPPC-C-PC	C Compiler - Windows/DOS
TSSPPC-C++-S1	C++ Compiler - Solaris 1.x
TSSPPC-C++-S2	C++ Compiler - Solaris 2.x
TSSPPC-C++-PC	C++ Compiler - Windows/DOS
TSSPPC-D-C-S1	C Debugger - Solaris 1.x
TSSPPC-D-C-S2	C Debugger - Solaris 2.x
TSSPPC-D-C-PC	C Debugger- Windows/DOS
TSSPPC-D-C++-S1	C++ Debugger - Solaris 1.x
TSSPPC-D-C++-S2	C++ Debugger - Solaris 2.x
TSSPPC-D-C++-PC	C++ Debugger - Windows/DOS

VME Development Systems

TVDS-SPARC-1
12 slot 6U VME enclosure, with Force 3CE SPARC based VMEbus master, 32 Mbytes RAM, ethernet, RS232 serial port for terminal, Solaris 2.x

TVDS-SPARC-2
12 slot 6U VME enclosure, with Force 3CE SPARC based VMEbus master, 32 Mbytes RAM, Sbus GX graphics board, 1Gbyte SCSI Disk, ethernet, RS232, keyboard, mouse, 17" monitor, Solaris 2.x RTU license

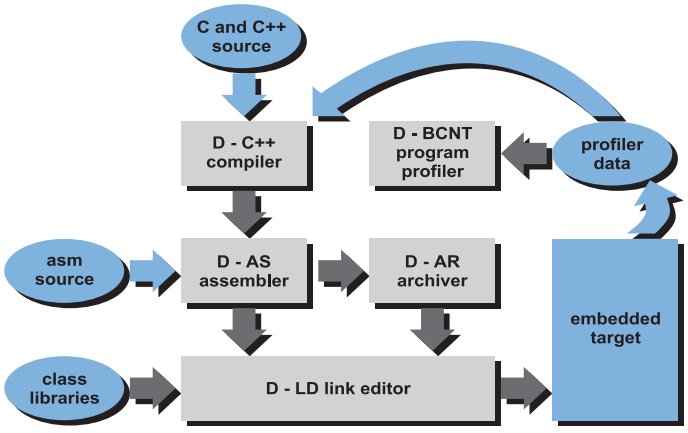


PowerPC C/C++ Compilers

Diab Data's C and C++ compilers are used for code development for Transtech's PowerPC products. PowerPC development benefits from state-of-the-art optimizations including superior inter-procedural register allocation, in-lining, and reaching analysis. This, together with PowerPC specific optimizations allows for the generation of extremely fast and compact code. The C-compiler conforms fully to the ANSI C X3.159-1989 standard and it includes, an optimized ANSI C Library with processor specific optimizations. The C libraries are also designed to be compliant with ANSI/ISO, POSIX and SVID standards. The C++ compiler is a complete implementation of the C++ language as described in ARM and ANSI drafts. The C++ is a true C++ compiler and is also source compatible with Cfront 2.1 and 3.0.

Profiler

The advanced program and source level profiler dynamically measures the program and monitors the source code as it executes in order to help the programmer understand and tune code execution. The profiler finds frequently used code and feeds the information back to the programmer, ensuring that compiler optimizations can be perfectly tuned to speed up the code where an application spends most of its execution time.



Assembler

The assembler performs fast assembly of compile output and supports conditional assembly as well as long symbol names and producing complete output listings for easy debugging and better program maintenance.

Linker

The linker performs incremental links, link optimizations and automatically searches archives for missing symbols.

Archiver

The archiver groups multiple files together in one archive file, and manages a database of symbols from object files in the archive.

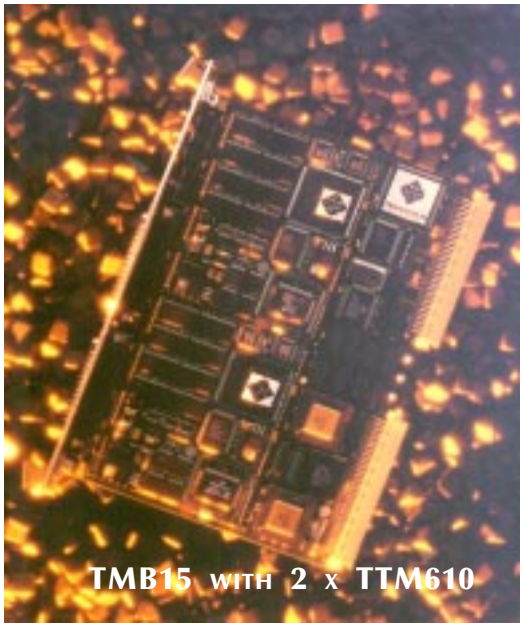
Code Optimizations

- global argument address assignment across functions
- register allocation across functions: a register not used in a called function is remembered across the call without having to be saved and restored
- common sub-expression elimination throughout an entire function, not just within a basic block
- register allocation and common sub-expression elimination interact to optimize them both simultaneously; without this functionality, each optimization could greatly reduce the benefits of the other, or even cause the other to generate worse code than if no optimization had been done
- delayed register saving: flow analysis of an entire function generates the code to save a register only when the register is first used, not on entry
- complex branch optimization, including substitution of branch instructions for the flag variables common in "goto-less" programming
- partial in-lining based on an execution profile; for example, the if-tests often used to immediately exit a function due to null arguments can be expanded in the caller, avoiding execution of the call, the return, and any register saves and restores
- functions which can never return, such as error abort or exit functions, can be marked by the user or automatically detected, with consequent elimination of register saving and other code.

Optimizations specific to the PowerPC

- code re-ordering and instruction scheduling based on flow analysis of entire functions; this maximizes pipelining for each PowerPC processor
- use of the count registers as for and while loop counters; this reduces overhead during the execution of loops
- early calculation of condition codes; this reduces PowerPC branch speculation

Other optimization techniques include register allocation using coloring, constant propagation and folding, operator strength reduction, redundant load/store elimination, loop invariant code motion and unrolling, common tail elimination, cascaded jump removal, dead code elimination, function inlining and many others


TMB15 with 2 x TTM610

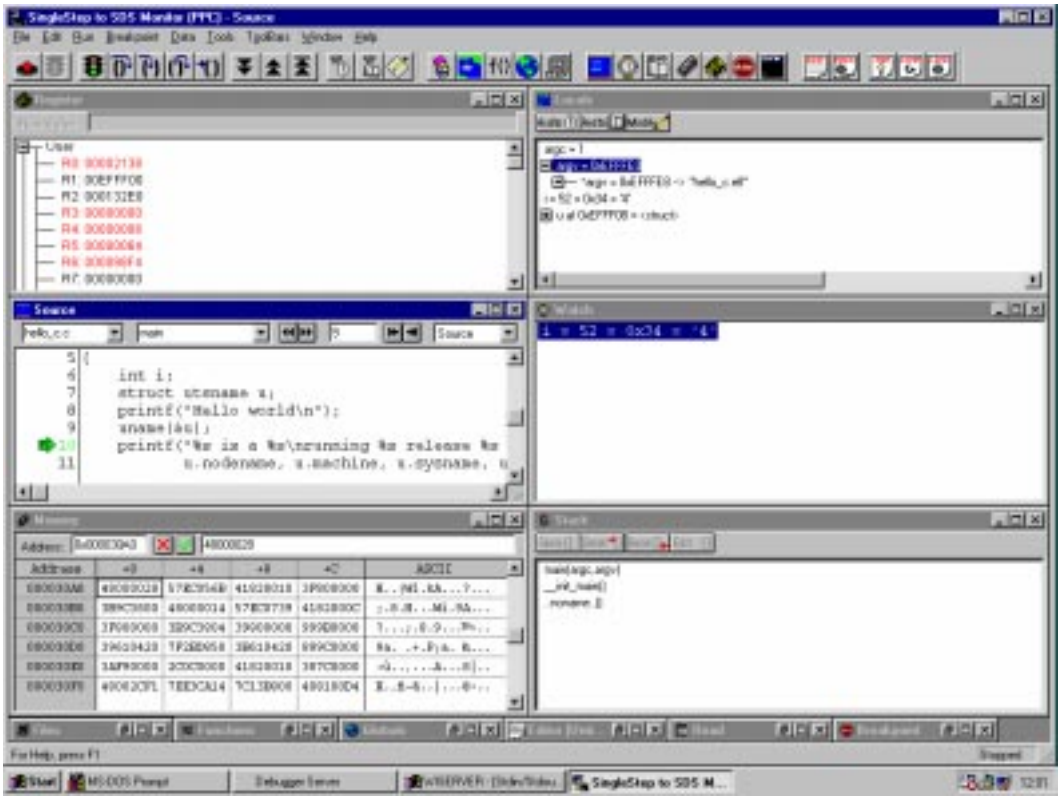
SingleStep C/C++ Debugger Features

- Easiest to use and most powerful user interface
- Debugs optimized C and C++ code
- Tightly coupled to Diab Data compilers for PowerPC
- Supports ELF/DWARF & PowerPC EABI standards

Debugging PowerPC C/C++ Code

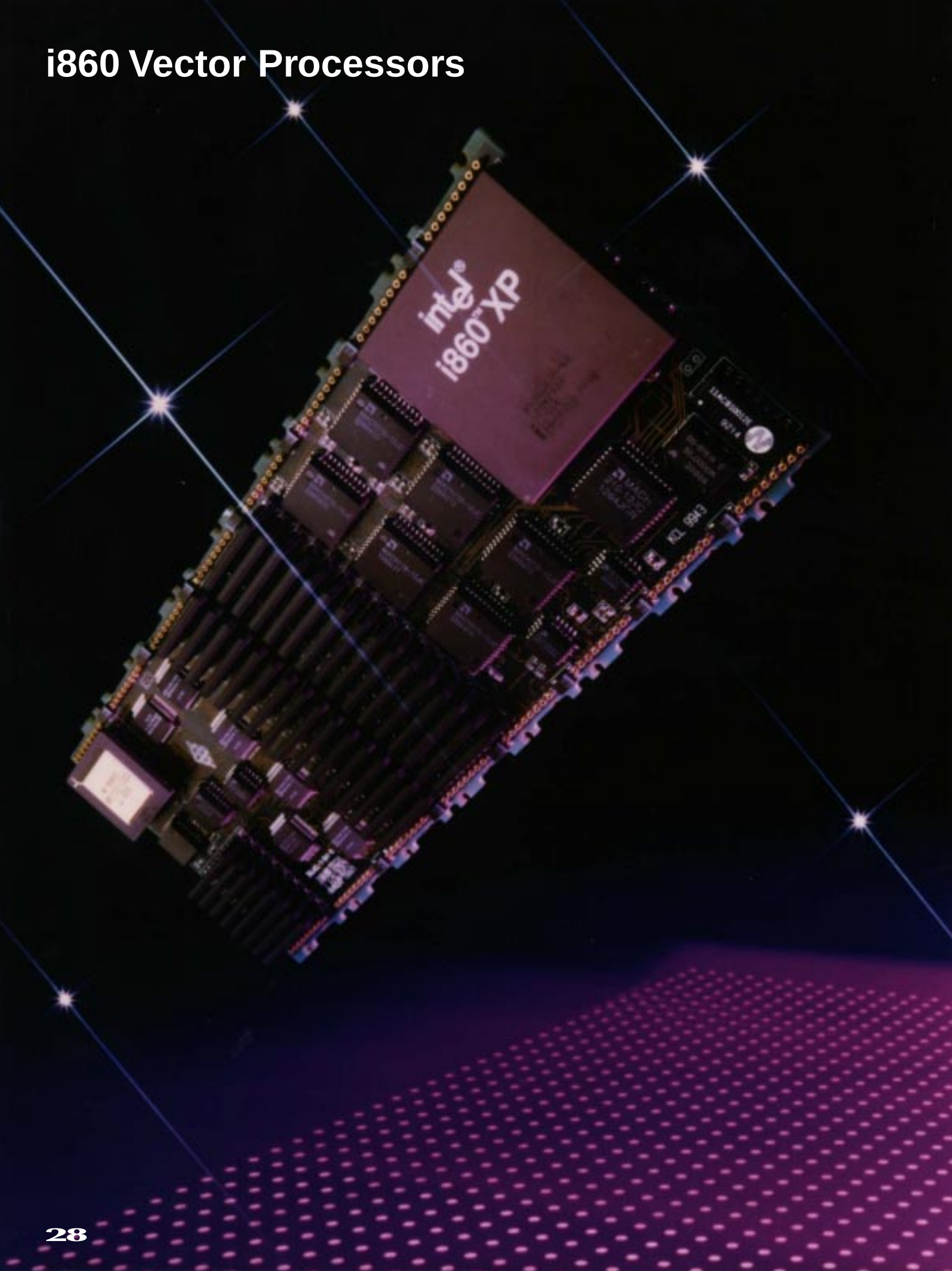
SingleStep from Software Development Systems (SDS) lets the user develop real time software faster than ever before. It is an open development and real time debugging environment that's easy to understand, easy to use and incredibly powerful.

Conforming to open standards such as ELF/DWARF and the PowerPC EABI, **SingleStep** can be tightly coupled to compiler packages such as those from Diab Data's thereby providing a highly integrated compiler/debugger environment with full source-level debugging in C and C++. It is this tightly coupled combination that provides the most powerful debugging environment for PowerPC. Also, since it offers a well designed GUI front-end that requires virtually no learning curve. The **SingleStep** target monitor allows debugging in real-time right on the target hardware.



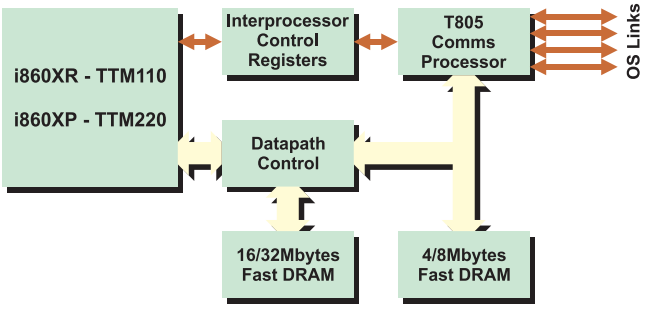
The **SingleStep** C and C++ debuggers are available for a number of platforms including Windows, Windows NT and Solaris.

i860 Vector Processors



TTM110 / TTM220

i860 Vector Processing TRAMs



TTM110 & TTM220 Block Diagram

The TTM110 is a size 6 TRAM module and has a shared memory architecture with 16 Mbytes of 64-bit wide fast DRAM coupled to both an Intel i860XR vector processor, and aT805 transputer to handle I/O and board-to-board communications via four 20Mbit/second serial links. The transputer has 4 Mbytes of private local memory. The two processors exchange data in shared memory, with interrupts and full bus locking for synchronization. The i860XR's memory controller supports sustained data transfer rates in excess of 100Mbytes/sec for pipelined read or write cycles. Peak performance of the TTM110 is 80MFLOPs.

TTM220 is a size 8 TRAM and also has a shared memory architecture with 16 or 32 MByte of 128-bit wide fast DRAM coupled to both an Intel i860XP vector processor, and an SGS-Thomson T805 transputer. The T805 handles I/O and board-to-board communications via four 20Mbit/second serial links. The transputer also has 4 or 8 Mbytes of private local memory. The two processors exchange data in shared memory, with interrupts and full bus locking to synchronize such transactions. The i860XP's memory controller fully supports burst transfers and data rates of up to 393Mbytes/second continuously for pipelined read or write cycles.

The TTM220 incorporates three innovative features (read caching, snoop filtering and write posting) that maximize shared memory bandwidth. Bus snooping can be disabled for applications where the fixed overhead of cache flushing prior to or following data exchange in shared memory is preferable to the variable overhead of snooping. The TTM220 utilizes the i860XP's MESI (Modify Exclusive Shared Invalid) ensuring cache and memory coherency between the shared memory and the i860XP's cache.

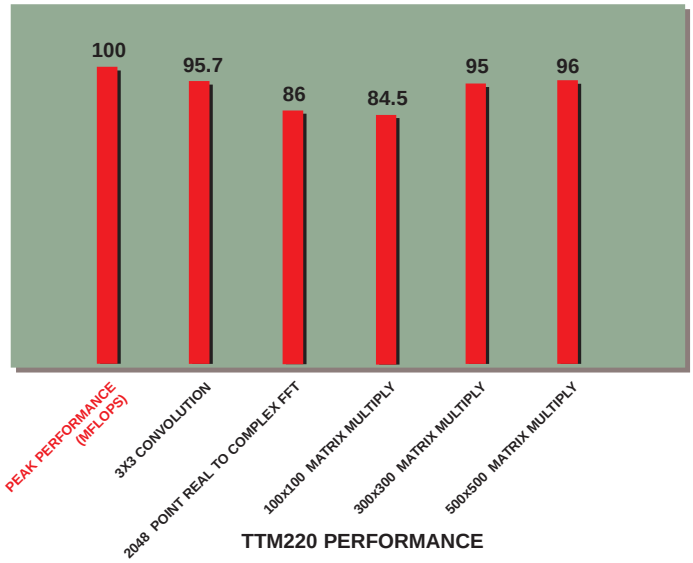
- **i860XR @ 40 MHz or i860XP @ 50 MHz**
- **Industry standard format (size 6 / 8 TRAM)**
- **16 or 32 MByte memory options**
- **T805 communications processor**
- **Compatible with TRAM motherboards**

ORDERING INFORMATION

TTM110-16/4	**i860 XR, 16 MByte version**
TTM220-16/4	**i860 XP, 16 MByte version**
TTM220-32/8	**i860 XP, 32 MByte version**

i860 Toolset

Software for TTM110 / TTM220



The software development environment for the TTM110/ 220 Series contains compiler technology from The Portland Group and a parallel run-time environment called the *i860 Toolset*. The Portland Group compiler tools, widely regarded as giving the best performance for the i860, include:

- ❖ Optimizing C and FORTRAN77 compilers
- ❖ Symbolic debugger
- ❖ Profiler

The profiler analyses data generated during execution of a specially compiled program, allowing users to discover which functions and lines of code were executed and how much CPU time they consumed. This is particularly useful when performance tuning' parallel applications.

The Transtech i860 Toolset provides a development and run-time environment for the TTM110/220 series modules. The Toolset may be purchased in a number of modules, the different levels supporting all systems from a PC/AT hosting a single TTM110 through to a networked supercomputer, comprising hundreds of TTM220s with dedicated peripherals and custom I/O facilities.

The basic framework of the i860 Toolset provides a run-time environment including host I/O services, assembler, loader, utilities, and memory management. Additional functionality available includes:

- ❖ BLAS (Basic Linear Algebra Subroutines)
- ❖ Signal Processing Libraries
- ❖ Inmos C Toolset

ORDERING INFORMATION

TSS860T-PC	**i860 Toolset**
TSS860T-S1	
TSS860T-S2	
TSS860C-PC	**C Compiler**
TSS860C-S1	
TSS860C-S2	
TSS860F-PC	**FORTRAN77 Compiler**
TSS860F-S1	
TSS860F-S2	
TSS860D-PC	**Debugger**
TSS860D-S1	
TSS860D-S2	
TSS860P-PC	**Profiler**
TSS860P-S1	
TSS860P-S2	

Where: PC = PC hosted
S1 = SunOS 4 / Solaris 1.x host
S2 = Solaris 2.x host

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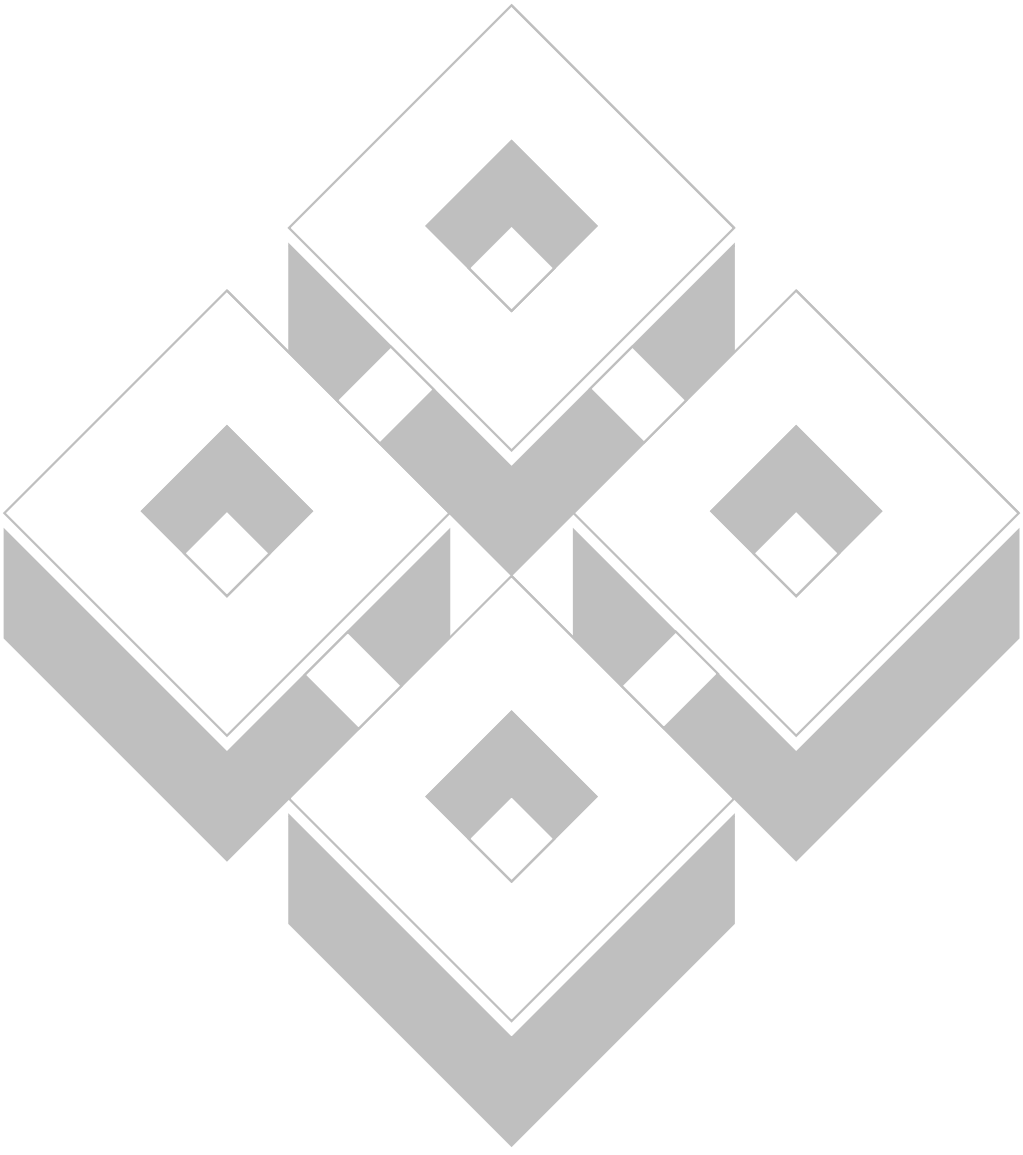

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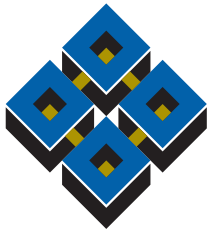

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