Initialization and Use of VIC068A/VIC64 Registers

At power up the VIC068A and VIC64 registers are automatically initialized to their most 'logical' state; the rule being not to prevent operation of the local processor, nor the VMEbus. This hardware initialization must be followed with a software initialization under local processor control to enable various functions of the VIC068A/VIC64.

The engineer can choose to initialize specific registers, or execute a complete initialization of the register set through a program loop associated with an indexed data table. The initialization phase does not prevent further modification of some registers, whose value is application-specific, not yet known at initialization time.

The first section of this document lists the VIC068A/VIC64 registers by increasing address, and gives a brief description of their functions (a detailed presentation is included in the Cypress *VMEbus Interface Handbook*). The second section groups VIC068A/VIC64 functions into categories and describes the associated registers.

Addresses, Functions, and Formats of Internal Registers

Reading/writing data from/to registers uses LD[7:0]. Addresses indicated hereafter are referenced using a byte-addressing format. Values in the Format column indicate the state of the register fields after Global Reset.

Table 1. Internal Registers

Register	Address (hex)	Function	Format
			7 6 5 4 3 2 1 0
VIICR	03	Enables/Disables local signaling of VMEbus IRQ acknowledge cycles, and associated IPL level.	1 1 1 1 1 0 0 0 0/1 : enable/disable IPL level
VICR 1–7	07–1F	Enables/Disables local signaling of VMEbus IRQs, and associated IPL levels.	1 1 1 1 1 0 0 0 0/1 : enable/disable IPL level
DMASICR	23	Enables/Disables local signaling of DMA interrupt on completion, and associated IPL level.	1 1 1 1 1 0 0 0 0/1 : enable/disable IPL level
LICR1–7	27–3F	Enables/Disables local signaling of LIRQs, triggering conditions, and associated IPL levels.	1 0 0 0 X 0 0 0 polarity IPL level 0/1 : level/edge (read) LIRQi status 0/1 : ext./int. ID vector 0/1 : enable/disable
ICGSICR	43	Enables/Disables local signaling of Global Switch activation, and associated IPL level.	1 1 1 1 1 0 0 0 Switch3 Switch2 Switch1 Switch0 0/1 : enable/disable IPL level
ICMSICR	47	Enables/Disables local signaling of Module Switch activation and associated IPL level.	1 1 1 1 1 0 0 0 Switch3 Switch2 Switch1 Switch0 0/1 : enable/disable IPL level

Table 1. Internal Registers (continued)

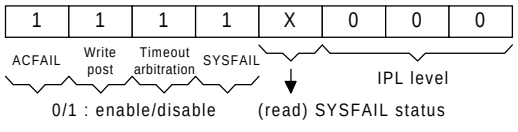
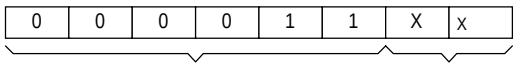
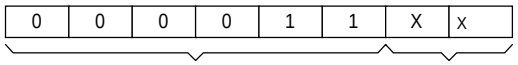
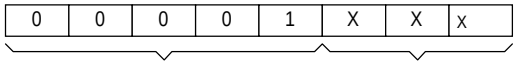
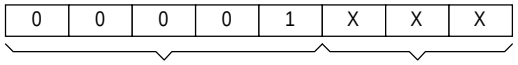
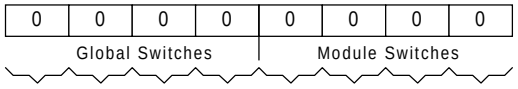
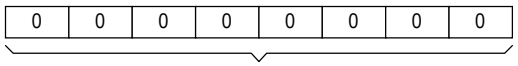
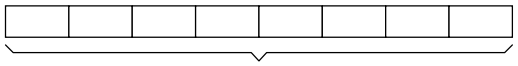
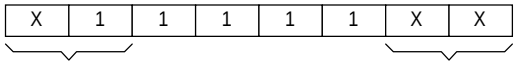
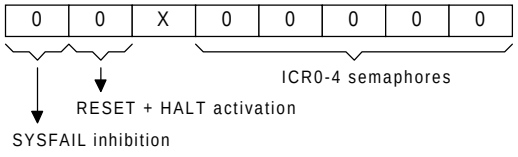
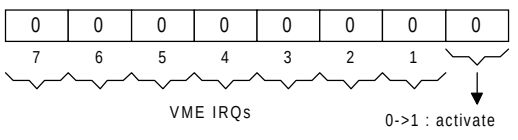
Register	Address (hex)	Function	Format
EGICR	4B	Enables/Disables local signaling of error group interrupts, and associated IPL level.	
ICGSVBR	4F	Local ID vector for Global Switches.	
ICMSVBR	53	Local ID vector for Module Switches.	
LIVBR	57	Local ID vector for LIRQs.	
EGIVBR	5B	Local ID vector for error group interrupts.	
ICSR	5F	Global and Module Switches access register.	
ICR0–4	63–73	General purpose Interprocessor Communication Registers.	
ICR5	77	VIC068A/VIC64 revision level.	
ICR6	7B	Halt & Reset status.	
ICR7	7F	Reset control, and semaphores for ICR0–4 registers.	
VIRSR	83	VMEbus IRQs activation and status.	

Table 1. Internal Registers (continued)

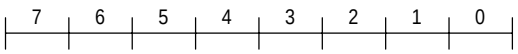
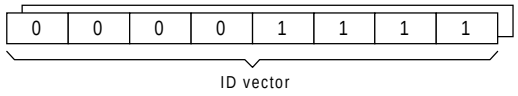
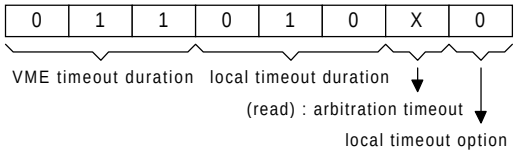
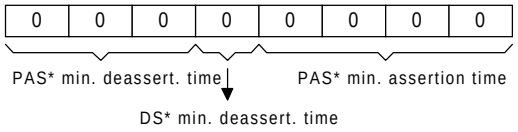
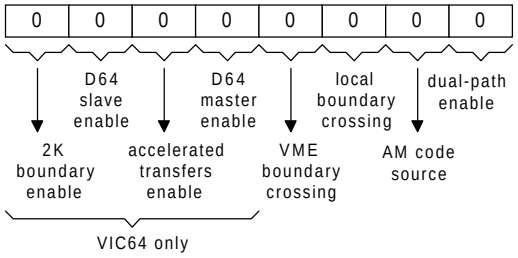
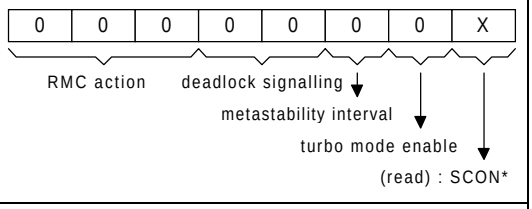
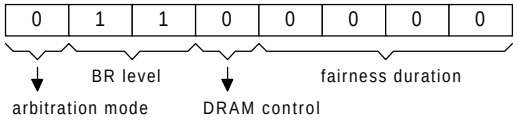
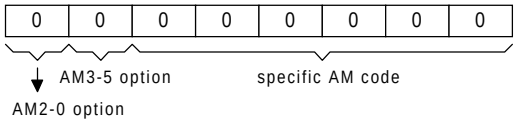
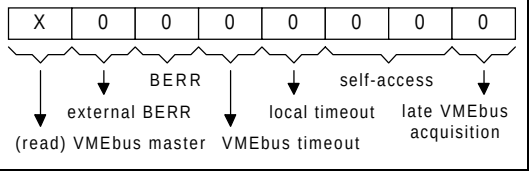
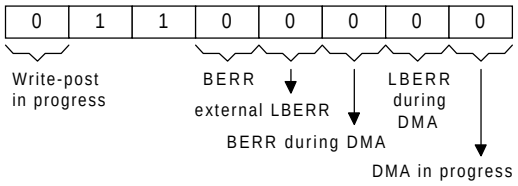
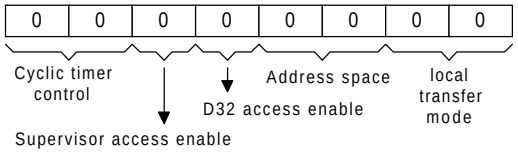
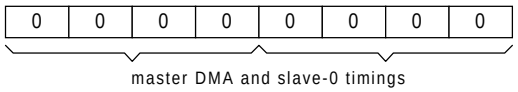
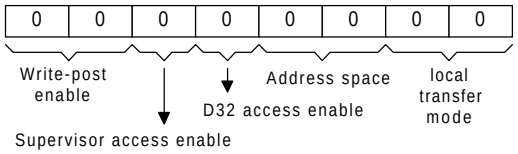
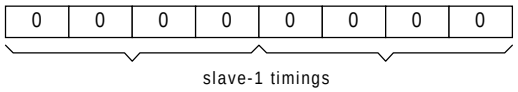
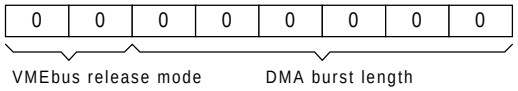
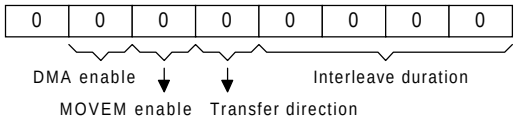
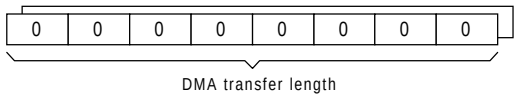
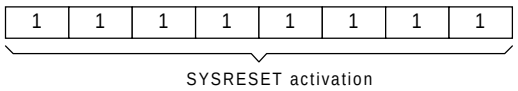
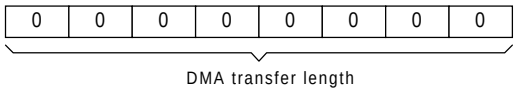
Register	Address (hex)	Function	Format
			
VIVBR1–7	87–9F	VMEbus IRQs ID vectors.	
TTR	A3	Transfer timeout conditions and values.	
LBTR	A7	Local bus timing.	
BDTR	AB	Block transfer conditions.	
ICR	AF	Various controls.	
ARCR	B3	Arbitration and Bus Request control.	
AMSR	B7	Specific AM codes.	
BESR	BB	Bus Error status.	

Table 1. Internal Registers (continued)

Register	Address (hex)	Function	Format
DMASR	BF	DMA transfer status.	
SS0CR0	C3	Control register #0 for slave #0.	
SS0CR1	C7	Control register #1 for slave #0 and master timings.	
SS1CR0	CB	Control register #0 for slave #1.	
SS1CR1	CF	Control register #1 for slave #1.	
RCR	D3	Burst length for block transfers, and VMEbus release mode.	
BTCR	D7	Block transfer parameters.	
BTLR1–0	DB–DF	Total block length (in bytes), LSB in BTLR0, MSB in BTLR1.	
SRR	E3	SYSRESET activation (on ‘F0’ write).	
BTLR2	E7	Block length extension (VIC64 only).	

Register Initialization by Function

The VIC068A/VIC64 registers are mapped into seven categories: Hardware Environment, Interrupts, System Controller, VMEbus Requester, Master Single Cycles, Master Block Transfers, and Slave Transfers. Within each category, associated registers have to be initialized before the associated functionality may be used.

Hardware Environment Registers

These register fields need to be correct for proper operation of the board in the system. If their default value does not comply with board architecture and configuration, they have to be overwritten before use of the associated functions.

TTR Register (A3)

bits 4–2, 0: Local bus timeout. The VIC068A/VIC64 can optionally monitor local bus cycles (including cycles in which it does not participate), and activate LBERR* in case of a timeout. Default state is 'no timeout control'.

LBTR Register (A7)

bits 7–5, 4, 3–0: Local bus timing. Defines the minimum duration of PAS* and DS* signals when the VIC068A/VIC64 is the local bus master (slave accesses or DMA transfers). Default state selects the shortest duration, i.e., the fastest timings.

BDTR Register (AB)

bit 5: (for VIC64 only) Enhanced turbo mode: setting this bit reduces the DSACK to DTACK delay by 1/2 CLK64M period. Default state is 'no turbo'.

bits 3, 2: Enable local and/or VMEbus boundary crossing. Boundary crossing during a block transfer is possible if and only if external address counters are implemented (such counters exist in the VAC068A controller and in the CY7C964 transceivers). Default state is 'no boundary crossing'.

bit 0: Enables Dual-Path. Dual-Path function allows for the VIC068A/VIC64 to execute single master accesses on the VMEbus during an interleaved block transfer, provided there is a dedicated path (for data and address) external to the VIC068A/VIC64. Such logic is implemented in the VAC068A controller and in the CY7C964 transceivers. Default state is 'no dual-path'.

ICR Register (AF)

bits 7–5: Define RMC* signal operation. The RMC* input signal may be used in different ways, e.g., VMEbus acquisition and hold until RMC* is released. Default state is 'RMC unused'.

bits 4–3: Deadlock signaling. A deadlock occurs when the VIC is requesting the VMEbus due to a local access and the VMEbus master is addressing the VIC068A/VIC64 as a slave. The deadlock may be reported through different signals depending on the values of bits 4-3. The resolution requires the local processor to temporarily release the local bus for VMEbus slave cycle execution. Default state is 'deadlock reported on DEDLK* signal only'.

bit 2: Metastability delay interval. The VIC068A/VIC64 executes a double sampling of asynchronous input signals, to prevent any internal metastability. The default interval is 3 periods, and can be extended to 4 by setting ICR bit 1.

bit 1: Turbo mode. When set, this bit accelerates VMEbus transfers by reducing timing phases by one CLK64M clock period. This mode is not recommended when the board has to operate in a standard VMEbus environment.

ARCR Register (B3)

bit 4: Enables DRAM refresh. Default is 'no DRAM.'

SS0CR0 Register (C3)

bits 7, 6: Enable periodic local interrupt enabling. The VIC068A/VIC64 can generate, on LIRQ2*, a cyclic signal of 50, 100 or 1000 Hz. This signal can be used by the local hardware, or directly generate a local periodic interrupt, by enabling LIRQ2 interruption. Default state is 'no periodic interrupt'.

bits 1, 0: Define local transfer type for accesses to slave-0. Default value is 'no access authorized to slave-0.'

SS0CR1 Register (C7)

bits 7–4, 3–0: Define local timings for slave-0 accesses, and DMA accesses. Default value selects the fastest timings.

SS1CR0 Register (CB)

bits 7,6: Enable Write posting for master and/or slave mode. Default state is 'no write posting.'

bits 1-0: Define local transfer type for accesses to slave-1. Default state is 'no access authorized to slave-1.'

SS1CR1 Register (CF)

bits 7–4, 3–0: Define local timings for slave-1 accesses. Default state selects the fastest timings.

ICR6 Register (7B)

bit 6: Reset detection and SYSFAIL* activation. Any Reset (Global, System or Internal) sets bit 6 of ICR6, which in turn activates the VMEbus SYSFAIL* signal. SYSFAIL* release is under software control, by resetting bit 6 of ICR6. This release is usually done after successful execution of local tests.

ICR7 Register (7F)

bit 7: SYSFAIL* inhibition. When reset (default state on Global or System Reset), this bit enables further SYSFAIL* signaling after

any Reset (Global, System or Internal). When set, SYSFAIL* will be signaled on Global or System Reset, but not after Internal Reset. This bit is usually set along with ICR6 bit 6 reset.

Associated with Interrupts (Local and VME)

The default state of all conditions mentioned hereafter is 'disabled'.

VIICR (03), DMASICR (23), EGICR (4B): Triggering and local signaling conditions for various interrupts.

EGIVBR (5B): Local ID vector for these interrupts.

VICR1–7 (07–1F): Triggering and local signaling conditions for VMEbus IRQs. The associated ID vector is obtained by execution of a local FCI-ACK cycle, automatically propagated onto the VMEbus by the VIC068A/VIC64.

LICR1–7 (27–3F): Triggering and local signaling conditions for LIRQIs.

LIVBR (57): Local ID vector for these interrupts.

ICGSICR (43), ICMSICR (47): Triggering and local signaling conditions for global switches and module switches.

ICGSVBR (4F), ICMSVBR (53): Local ID vectors for these interrupts.

VIRSR (83): Activation and status of VMEbus IRQs.

VIVBR1–7 (87–9F): VMEbus ID vectors for IRQs. These vectors are presented by the VIC068A/VIC64 on IACK VMEbus cycles.

Registers Associated with System Controller Functions

TTR Register (A3)

bits 7–5: VMEbus timeout duration. During VMEbus cycles BERR* will be activated when no answer from slave (DTACK* or BERR*) is obtained after this limit. Default value selects the shortest timeout (4us).

ARCR Register (B3)

bit 7: Arbitration mode for VMEbus Bus Requests. Selecting Round-Robin mode (default) gives each BR level the same average priority. When selecting Priority mode, the VIC068A/VIC64 serves lower levels only when no request is pending on a higher level.

Registers Associated with VMEbus Requester Functions

ARCR Register (B3)

bits 6–5: VMEbus request level. Default level is BR3.

bits 3–0: Fairness duration. The VIC068A/VIC64 can adopt a polite behavior when requesting VMEbus mastership, by waiting until its BRx* level is inactive before to do so, meaning that no other requester, especially further down the daisy-chain, is waiting for service. The fairness duration is adjustable, when exceeded the VIC068A/VIC64 automatically requests the bus. Default state is 'Fairness disabled'.

RCR Register (D3)

bits 7–6: VMEbus release mode. Release-When-Done is usually selected in multi-master environments, where bus mastership frequently hops from one master to another. Release-On-Request (default) is preferred in single-master environments, or in multi-master environments with a dominating master. Release-On-Bus Clear is used in strict priority-oriented environments. Finally, VMEbus-Capture-and-Hold is used when bus mastership has to be retained.

Registers Associated with Master Single Transfers

AMSR Register (B7)

bits 7, 6, 5–0: Specific AM code. AM code generation depends on the ASIZ1/0 local signals state: usually the AM code is generated automatically, but if both ASIZ signals are low the AM code is provided by AMSR register. This register can also define a specific AM code for block transfers or slave transfers.

Registers Associated with Master Block Transfers

BDTR Register (AB)

bit 4: (VIC64 only) Enables D64 block-transfers for master accesses. Default state is 'D64 block transfers disabled'.

bit 1: Defines whether the AM code for block-transfers is standard (automatically generated by the VIC068A/VIC64) or issued from AMSR register. Default state is 'standard AM code'.

AMSR Register (B7)

(see above)

RCR Register (D3)

bits 5–0: Bursts length, defined in number of VMEbus cycles (not bytes). For the VIC64 the actual number of cycles will be four times the register value. Default value is 64 cycles/burst (VIC64: 256 cycles/burst).

BTCR Register (D7)

bit 6: Enables DMA transfer. Next assertion of MWB* will start the transfer. Default state is 'DMA transfer disabled'.

bit 5: Enables MOVEM transfer. Default state is 'MOVEM transfer disabled'.

bit 4: Transfer direction. Default is 'Write'.

bits 3–0: Interleave duration for burst transfers. Default value selects the minimum duration (250 ns).

BTLR2 (E7), BTLR1 (DB), BTLR0 (DF) Registers

Total transfer length, in number of bytes. LSBs in BTLR0. BTLR2 only used for VIC64.

Registers Associated with Slave Transfers

BDTR Register (AB)

bit 6: (VIC64 only) Enables D64 block transfers for slave accesses. Default state is 'D64 block transfers disabled'.

SS0CR0 (C3), SS1CR0 (CB) Registers

bit 5: Supervisor cycles accepted. Default state is 'no Supervisor cycles'.

bit 4: D32 cycles accepted. Default states is 'no D32 cycles'.

bits 3–2: Address Space configuration: A32, A24 (default), A16 or AMSR-defined.

Conclusion

The VIC068A and VIC64 are the most flexible VMEbus controllers available. A number of internal registers, must be configured to customize the functionality of the VIC068A/VIC64. These registers receive a default value at power-up and during reset. If desired, the default value can be overwritten, at the system or application initialization period. Registers involved in DMA transfers must be initialized on every launch.