

NEW T9000 PRODUCT INFORMATION

- New data is available covering the following :
- Instruction and Data Cache
Cache organization and configuration
Cache instructions and operation
- Data/Strobe Links
Link format and protocol
Handling errors on links
Link configuration and reset

T9000 RELEASE PHASES

- ALPHA RELEASE
Reduced functionality CPU
No VCP
- BETA RELEASE
ALPHA plus VCP
- GAMMA RELEASE
Fully functional CPU
Fully functional device

SPECIFICATION CHANGES

- The following are differences from previously published specifications
- Binary code compatibility with T805 is not being supported.
This is not really a problem.
- Devices mapped into PMI must now be mapped as a 'DEVICE'

COMMUNICATIONS & SYNCHRONIZATION

- T9000 supports zero length messages with 'in' and 'out' instructions
- 'variable in' 'variable out' & 'load count' allow for variable length message transfers.
- Many-to-one distributed communications supported by 'Resource channel mechanism'.

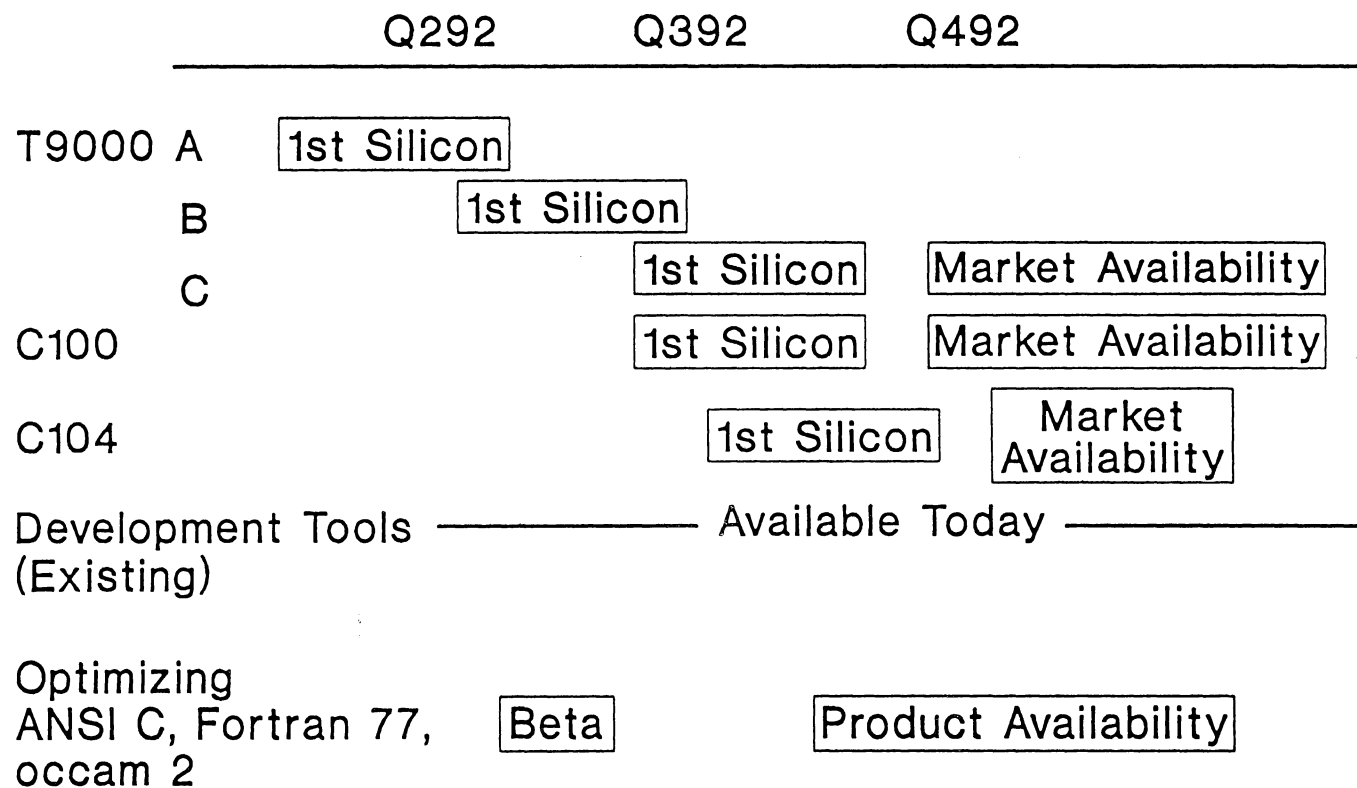
WILL INVOKE
A TRAP => HANDLER.
← COMPILER
DIRECTIVE

T9000 BETA SILICON

- The following will not be implemented on BETA silicon :
- **TIMESLICING**
The timeslice instruction will cause the current process to be ~~de~~-scheduled.
- **SINGLE-STEPPING & WATCHPOINTING**
This support for debugging will be fully functional on GAMMA release.
- **CRC & DEVICE ACCESS.**

*MMU APP'S
i.e. SEQ
OPERATION.*

T9000 Family Timescales



PROGRESS REPORT: (24-MAR-1992)

Block	Design	Layout	Layout Completion
CPU	100%	90%	April '92
FPU	100%	100%	Complete
Links	100%	100%	Complete
VCP	90%	80%	May '92
PMI	100%	100%	Complete
Cache	100%	100%	Complete
Control unit	100%	100%	Complete

T9000 PRODUCT FAMILY TIMESCALES:

Product	1st Silicon	Samples
T9 alpha	Jun 1992	Jul 1992
T9 beta	Jul 1992	Aug 1992
T9 gamma	Oct 1992	Nov 1992
C104	Oct 1992	Nov 1992
C100	Sep 1992	Oct 1992