

**IMS T424 transputer**

The IMS T424 is a 32 bit transputer providing 10 MIPS, with 4 Kbytes of static RAM, a 32 bit multiplexed memory interface, an 8 bit peripheral interface and four standard INMOS links.

**IMS T222 transputer**

The IMS T222 is a 16 bit transputer. It has an identical instruction set to the IMS T424 and programs will behave identically on both the T222 and T424, providing the 16 bit range of the T222 is not exceeded.

**IMS G213 graphics processor**

The IMS G213 is a high performance programmable graphics controller, suitable for high quality colour graphics. It includes a 16 bit processor, 2 Kbytes of static RAM and two INMOS links for connecting to transputer systems.

**IMS M212 disk processor**

The IMS M212 is an integrated programmable disk controller for floppy disks and Winchester. It includes software configurable crc/ecc, as well as a 16 bit processor, 2 Kbytes of static RAM and two INMOS links for connecting to transputer systems.

**Occam**

A simple high level language for both specifying and programming concurrent systems of one or more processors.

**Occam evaluation kit**

The occam evaluation kit is an electronic tutorial system for demonstrating the basic principles of occam.

**Occam programming system**

A personal workstation with 256 Kbytes of memory providing an initial programming tool for developing occam programs.

**inmos**<sup>TM</sup>

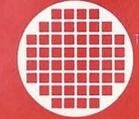


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**IMS T424  
transputer**

For design data refer to INMOS published Data Specifications from which these extracts are taken.



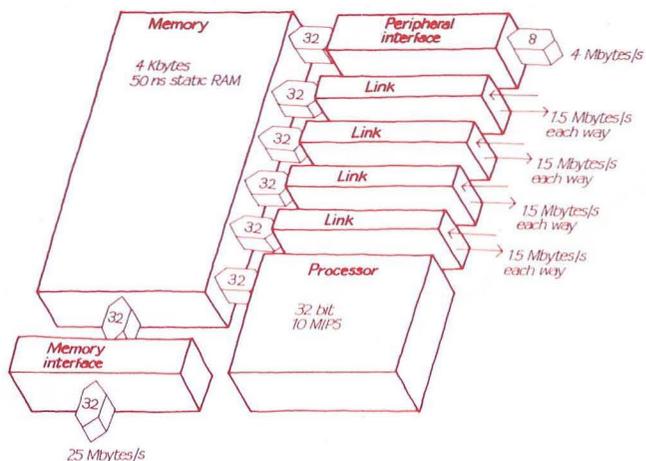
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The IMS T424 is the first of a range of transputer products which will span the entire spectrum of micro-processor applications, from low cost microcontrollers up to supercomputers and fifth generation systems. All transputers will be totally compatible, whatever their word length, instruction set, processor speed, or interfaces.

**IMS T424**

32 bit system providing 10 MIPS (millions of instructions per second) processing power with memory and concurrent communication capability, all on a single chip.

**Processor**

Reduced instruction set for compact programs, efficient high level language implementation and direct support of concurrency. High performance arithmetic with 50 ns basic instructions, 600 ns process switch and 950 ns multiplication.

**Memory**

4 Kbytes of static memory giving a maximum data rate of 80 Mbytes/s. Multiport access for processor, peripheral interface and each INMOS link.

**Memory Interface**

32 bit multiplexed interface, with programmable timing to support mixed memory systems. Extends direct address memory space up to 4 Gbytes with a maximum data rate of 25 Mbytes/s.

**Memory interface signals**

- Ras → Address valid
- Gas → Column address strobe
- Re → Read data enable
- We0-3 → Byte 0 to 3 write data valid
- Amux → Address multiplex
- AD0-31 ↔ Address/data
- Mcycle ← Multiplexed/non-multiplexed cycle select
- Await ← Asynchronous wait input

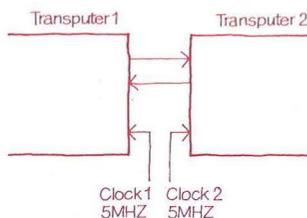
**Peripheral interface signals**

- Iclk ← Peripheral interface clock
- Req → Request for data transfer
- Ack ← Acknowledge data transfer
- I/O → Direction of transfer
- C0,1 → Which of four channels is being addressed
- D0-7 ↔ 8 bit wide data bus
- Event ← Event input to schedule a process

**Peripheral Interface**

8 bit bi-directional interface, providing connection to industry standard devices like controllers, processors and memory. Concurrent block transfer capability of 4 Mbytes/s.

**INMOS links**



Four INMOS standard serial links providing concurrent message passing capability to other transputer devices. Programmable data rate up to 1.5 Mbytes/s full duplex on each link to enable local and remote connection.

**Technology**

250,000 devices fabricated in an advanced 2 micron CMOS process, mounted in an 84 contact leadless chip carrier.

**Programming**

Programmable in most standard high level languages: Ada, Basic, C, PASCAL... Direct execution of occam for maximum performance and exploitation of concurrency. Interactive program development using occam as the lowest level image of the system.

**Performance**

		Program size (bytes)	Execution time (ns)
<b>Arithmetic operators</b>	+, -	1	50
	* (multiplication)	1	950
	/ (division)	2	1950
<b>Comparison operators</b>	>, <, <=, >=	2	100
<b>Logical operators</b>	AND, OR	1	50
	^, V, >< (xor)	2	100
<b>Shift operators</b>	<< [n], >> [n]	2	50n+50
<b>Identifiers</b>	variable	1.7	120
<b>Expression evaluation</b>	constant	1.3	70
	SEQ [n]	0	0
	PAR [n]	9n-7	450n-200
	ALT [n]	8n+7	600n+600
	IF [n]	3n	150n
	WHILE	4	200
<b>Primitives</b>	! (output), ? (input)	4	625
	! [n], ? [n] (vector)	4	50n+625
	:= (assignment)	0	0
	:= [n] (vector)	4	100n+300

The transputer is a high performance component when used in single transputer configurations. Pipelines and arrays of transputers can be used to provide greatly increased performance by exploiting the concurrency inherent in many applications.